Zero-Current-Switch Quasi-Resonant Boost Converter in Power Factor Correction Applications

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Abstract- A modified zero-current-switched quasi-resonant (ZCS-QR) boost converter is employed in a power factor correction (PFC) application. The main goal is to achieve a small-size low-noise PFC circuit based on single-switch boost topology. A clamp diode has been added to avoid the voltage ringing problem that is originally generated across the ZCS-QR switch during its turn-off period. The converter operation states after clamp diode application are presented. The PFC circuit control scheme implementation is also described. An experimental circuit with 100 V rms ac of 50 Hz input and 330 V dc output has been built. A high efficiency of 90% and the proof of compliance to the IEC61000-3-2 class D have been confirmed by experiment.

Key words: PFC, Boost Converter, ZCS-QR, single-switch

I. INTRODUCTION

Power factor correction (PFC) circuit becomes mandatory in off-line power application to comply with IEC61000-3-2. The standard specifies harmonics limit up to 39th and applies to most electrical equipment with input power greater than 75 W [1]. However, as most PFC circuits are implemented by power electronics approach, it should also pass the electromagnetic interference (EMI) standards such as EN50081 or CISPR Publication 22.

Incorporating a topology that generates as small EMI as possible could ease further EMI filtering effort. The zero-voltage-switched (ZVS) topology is characterized by that capability [2]. However, this solution normally employs more than one active switch if being applied into PFC application circuits [3, 4, and 5]. It leads to complex control scheme and high production cost.

Fig. 1. Conventional full-wave ZCS-QR boost topology

Fig. 2. v_s and i_{Lr} under severe ringing voltage

Providing other option; this paper presents a single-switch PFC incorporating full-wave zero-current-switched quasi-resonant (ZCS-QR) boost converter. Like its ZVS counterpart, ZCS topology is also known to generate less EMI [2, 6].

Interesting characteristics of the ZCS-QR solution while being applied to PFC applications are: (1) parasitic elements around converter would be less excited if compared to hard switching solution [6], (2) its inherent variable frequency control mechanism is capable to spread the EMI spectrum [7, 8]. Those points give positive effect to the EMI level reduction.

The proposed topology also has other advantage. This ZCS-QR PFC may be operated over higher switching frequency without sacrificing too much of its efficiency. High operating frequency condition leads toward smaller reactive components requirement. It results in less occupied space, weight reduction, and cheaper solution.

Fig. 3. Proposed full-wave ZCS-QR boost topology

Fig. 4. v_s and i_{Lr} after clamp diode D_c is added to the circuit

II. ZCS-QR BOOST PROBLEM AND SOLUTION

A conventional ZCS-QR boost converter is depicted in Fig. 1. In real application, the main switch S of that circuit has certain value of parasitic capacitance C_s . During S turn-off period, C_s and the resonant inductor L_r construct a parallel resonance circuit. At that moment, body diode D_s reverse recovery current excites the resonant circuit. This generates voltage ringing as depicted in Fig. 2.

This ringing condition may excite parasitic circuits around S . It results in higher EMI level of the PFC circuit.

The voltage ringing also forces designer to use higher voltage rating MOSFET. It is because the voltage level of that ringing may be very high; depend on the quality factor Q of the resonant C_s - L_r circuit.

In this work, a clamp diode D_c is added to the ZCS-QR circuit to alleviate the ringing problem. The modified circuit is shown on Fig. 3. Result of this modification on the key waveform of the ZCS-QR switch is depicted in Fig. 4.

Fig. 5. The proposed ZCS-QR boost topology key waveforms

Fig. 6. Operating states of the proposed converter

III. THE PROPOSED CONVERTER'S WORKING STATES

Fig. 5 depicts the proposed ZCS-QR boost converter key waveforms. The circuit operating conditions of that waveforms are $V_i=100$ V, $V_o=360$ V, $I_i=2.38$ A, $I_o=0.6$ A, and $f_s=128$ kHz. It can be inferred from that figure that the modified ZCS-QR boost converter could be divided into six operating states as shown on Fig. 6. a to f.

Fig. 6. a to d show similar working stages as in a conventional full-wave ZCS-QR boost converter. However, Fig. 6. e and f are specific to this proposed topology.

It could be seen from Fig. 6. e that D_c forces V_s be instantaneously equal to V_o during its turn-off period. This completely eliminates the voltage ringing possibility.

Fig. 6. f pointed out that during the last cycle, input inductor current (i_i) is divided into boost diode current (i_{Db}) and the clamp diode current (i_{Dc}). Therefore, it should be realized that this proposed topology is characterized by:

1. Zero-current-transition will be occurred during switch turn-off action as long as limit in (1) from [2] is fulfilled.

$$I_{i_max} = \frac{V_o}{\sqrt{\frac{L_r}{C_r}}} \quad (1)$$

2. Non-zero-current-transition will always be occurred during main switch turn-on action. This is caused by i_{Dc} (Fig. 5 waveform 5).

Fig. 7. Control block diagram of the proposed PFC circuit

3. i_{Dc} also make the D_c susceptible to reverse recovery current problem during transition from state 6 to state 1 (Fig. 5 waveform 9).

Point 2 and 3 limit the converter performance in term of losses, EMI emission, and its maximal operating frequency.

IV. THE PFC CONTROL SCHEME

A. Basic Control Technique

Reference [8] pointed out that the order of small-signal control to output characteristics a ZCS-QR converter is the same to a conventional hard-switched solution. This makes the well-proven multiplier-based current-averaged PFC control scheme become preferred control candidate.

Fig. 7 shows the block diagram of the proposed PFC circuit. This control scheme is based on commercially available PFC control circuit. It consists of two control-loops; the inner current loop and the outer voltage-loop. For conventional hard-switched PFC circuit, all functions related to control circuit are normally contained inside a single chip IC. In this kind of IC, output of the average current controller is internally fetched to a PWM module.

Fig. 8. Input voltage and current of PFC 2

Fig. 9. Harmonic spectrum of current on Fig. 8

However, a ZCS-QR converter is controlled by frequency modulation instead of a PWM controller. Therefore, in the proposed PFC topology, the PWM module is bypassed and an external connection to a voltage-controlled oscillator (VCO) is made.

B. Current Amplifier Gain

In order to achieve current-loop stability, the amplified inductor current down slope must not exceed the oscillator ramp slope [10]. This criterion provides a mean to determine the optimal point of the current amplifier gain (G_{CA}) inside the I_i Compensator on Fig. 7. G_{CA} could be solved by (2).

$$G_{CA} = \frac{\hat{V}_{CA}}{\hat{V}_{RS}} = \frac{V_S f_s L_i}{V_O R_s} \quad (2)$$

$\hat{V}_{CA}$ is the oscillator ramp slope, $\hat{V}_{RS}$ is the current-amplifier off-time slope. In PWM controller, V_S is the peak to peak ramp voltage while in ZCS-QR controller, V_S is the input voltage range of the VCO. f_s is the switching frequency, L_i is the input inductor, V_O is the output voltage, and R_s is current sense resistance.

It is realized from (2) that due to variable frequency operation nature of the ZCS-QR control technique, the current amplifier gain should also be variable. To simplify the overall design process, in this paper, the current amplifier gain is set to be fixed on the lowest switching frequency point. It means, the circuit control performance would be slightly deteriorated while the converter operates under high switching frequency.

TABLE I
PARAMETER LIST OF THE CONVERTERS

Parameter Name	PFC 1	PFC 2
L_i	600 μ H	200 μ H
C_o	330 μ F	330 μ F
L_r	100 μ H	22 μ H
C_r	10 nF	6.6 nF
V_i	100 V rms	100 V rms
V_o	270 V	330 V
$P_{i \max}$ ^{a)}	127 W	367 W
Controller minimum frequency	35 kHz	100 kHz
Controller maximum frequency	140 kHz	350 kHz

^{a)} real circuit maximum input power where ZCS condition still occurs

Fig. 10. Total harmonic distortion comparison between PFC 1 and PFC 2

C. Current Compensator Pole and Zero Placement

In order to determine the position of pole and zero of the I_i Compensator, the cut-off frequency (f_c) should be found first. f_c could be solved by (3) [10].

$$f_c = \frac{f_s}{2\pi} \cdot \frac{1}{D} \quad (3)$$

D is the duty cycle. In a ZCS-QR converter, a variable called μ is used as the equivalent value of D . μ could be found by (4) [11].

$$\mu = f_s \cdot (2\pi \sqrt{L_r C_r}) \quad (4)$$

f_c position for the ZCS-QR topology could be determined by substituting (4) into (3). Therefore, pole and zero placements could be determined by:

$$\text{zero} = \frac{f_c}{2} \bigg|_{f_{s_min}} \quad (5)$$

$$\text{pole} = f_{s_min} \quad (6)$$

f_{s_min} is the minimum switching frequency of the VCO.

D. Outer-Loop Configuration

Procedure stated on [12, 13] has been followed in order to solve the outer loop parameter calculation.

Fig. 11. Efficiency comparison between PFC 1 and PFC 2

Fig. 12. Conducted EMI test of PFC 2

Two PFC circuits have been made to examine the real circuit characteristics and performance. Parameters for both PFC circuits are listed in table 1. The control parameters have been optimized individually to each converter based on calculation scheme mentioned on section IV.

V. CIRCUIT PERFORMANCE

Fig. 8 shows the input voltage and current waveform of the PFC 2. The current waveform is further analyzed to acquire its harmonic contents. Its harmonics histogram is depicted in Fig. 9. This figure shows that the input current passes the IEC61000-3-2 class D standard.

Further examination on the total harmonic distortion (THD) performance of both converters could be evaluated from Fig. 10. It could be seen that minimum THD could be achieved when converters operates about 50% to 60% of its maximum power. This phenomenon requires further investigation in order to achieve as low THD as possible during all operating condition.

Fig. 11 explains about the converters efficiency. It is shown that PFC 1 provides better efficiency compared to PFC 2. It is because PFC 1 is operated under smaller output voltage and slower switching frequency.

In term of efficiency, both PFC circuits have the same tendency to gain highest efficiency while being operated near its maximum input power condition. This confirms the nature of ZCS-QR circuit that is characterized by low efficiency while lightly loaded.

EMI characteristic measurements also have been done. Fig. 12 shows EMI signature of the PFC 2, without any input filter, 100 V input voltage, 330 V output voltage, and 449 Ω load. From the figure it is revealed that less EMI is generated by the PFC circuit, especially in high frequency region over 1 MHz, when it is operated as a PFC. Therefore, the inherent frequency modulation control in the PFC circuit gives potency to reduce its noise signature in high frequency region.

VI. CONCLUSION

A ZCS-QR boost converter has been incorporated in a PFC circuit. With only a minor modification to the conventional PFC control circuit, compliance to the IEC61000-3-2 harmonics standard has been achieved. Reasonably high efficiency could be achieved. However, higher output voltage and faster switching frequency could suffer the converter efficiency. Potential to EMI reduction in high frequency spectrum also has been confirmed. Further investigation regarding optimization of the control technique and EMI reduction should be done.

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