Steady State Characteristics of Active-Clamped Full-Wave Zero-Current-Switched Quasi-Resonant Boost Converters

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Abstract- **This proposed boost converter utilizes active-clamp circuit to achieve zero-voltage-switched (ZVS) transition in a full-wave zero-current-switched quasi-resonant (ZCS-QR) converter. The ZCS-ZVS switching transition results in higher efficiency, better output voltage regulation, opens possibility to incorporate higher switching frequency, and has some potency to reduce converter's conducted EMI. It is important to note that the active-clamp circuit works under ZVS condition. Therefore, this switch will not cause excessive losses and extra EMI. In this paper, the working principle and steady state performance of the proposed boost converter are presented. A 100 V dc input, 300 W maximum output, and 430 kHz resonant frequency experimental circuit has been built. Maximum efficiency of 95.6% has been confirmed by experiment.**

Index Terms: active clamp, boost converter, full-wave ZCS-QR, ZVS

I. INTRODUCTION

Boost converter is normally applied to a power factor correction (PFC) circuit for its high performance and simplicity [1]. However, its hard-switching nature rise some issues related to reverse recovery of the catch diode, main switch parasitic capacitance loss, and electromagnetic interference (EMI) problem.

This work is part of an effort in implementing PFC circuit based on full-wave zero-current-switch quasi-resonant (ZCS-QR) technique as an alternative to conventional boost-based PFC. The ZCS-QR technique has been chosen as it is claimed to generate less EMI and makes the implementation of higher switching frequency more feasible [2]. Instead of half-wave ZCS-QR, full-wave topology has been selected for its consistent timing consideration. This makes the converter control effort less demanding.
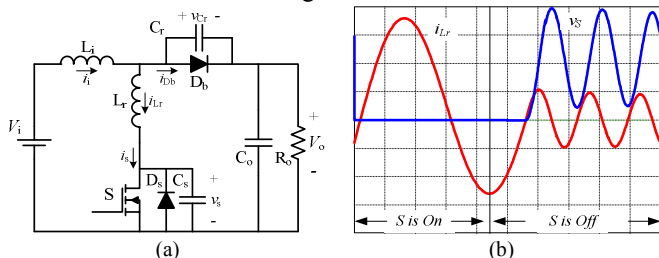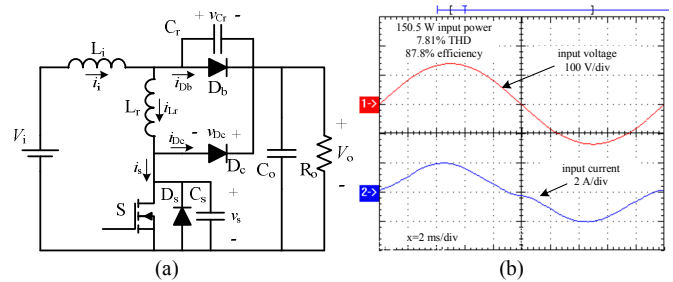

Fig. 2. (a) Diode-clamped full-wave ZCS-QR boost converter schematic diagram and (b) its performance while implemented as PFC circuit.

Fig. 1. (a) shows the schematic diagram of a conventional full-wave ZCS-QR boost converter. In real application, the main switch S experiences severe voltage ringing during its turn-off period. This ringing is caused by resonant condition of the switch parasitic capacitance C_s and the series resonant inductance L_r. Reverse recovery current of anti-parallel diode D_s excites this resonant circuit and induces voltage ringing as shown on Fig. 1. (b).

A clamp diode D_c has been added to the circuit like shown on Fig. 2. (a) to avoid the ringing problem. The clamped circuit performs well while being implemented as a PFC. The input current waveform of the PFC is depicted in Fig. 2. (b) [3].

After D_c has been added to the full-wave ZCS-QR boost converter, switch waveform is free from ringing (Fig. 3. (a)). However, the figure reveals additional troubles those are: (a) high reverse recovery current occurs on D_c and (b) i_{Lr} is non-zero during switch turn-on transition. Those problems result in higher losses and more EMI emission.

Fig. 1. (a) The schematic diagram of a conventional full-wave ZCS-QR boost converter and (b) its v_s and i_{Lr} waveforms under severe ringing voltage.
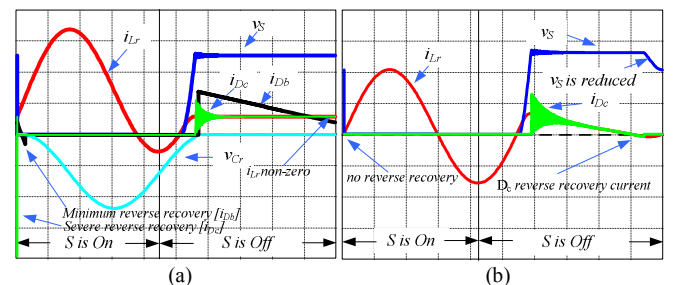

Fig. 3. Diode-clamped full-wave ZCS-QR boost converter's waveforms under very light load condition
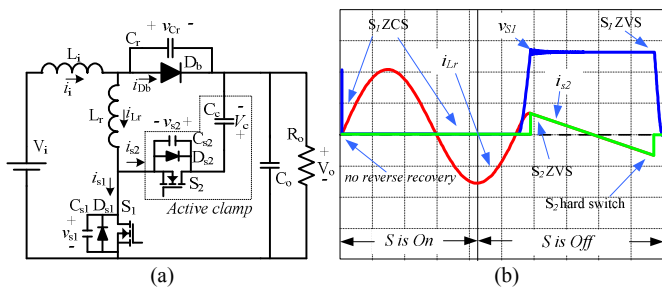
Fig. 4. (a) The schematic diagram of an active-clamped full-wave ZCS-QR boost converter and (b) its key waveforms.

Fig. 3. (b) shows the diode-clamped topology key waveforms while being lightly loaded. It can be seen that the switch voltage v_S is slightly reduced after reverse recovery current of D_c ceased. This behavior is similar to an active-clamped technique.

Active clamp technique is known for its capability to avoid voltage ringing while also give additional zero-voltage-switch (ZVS) transition benefit [4]. Therefore, formally applies this technique to a ZCS-QR boost converter results in a ZVS-ZCS switching action.

Theoretically, ZVS-ZCS switching action eliminates switching losses and significantly reduces the electromagnetic interference (EMI) level. Those return in possibility to further increase the converter switching frequency in order to achieve circuit miniaturization while maintaining efficiency.

Furthermore, less filtering effort is required to fulfill the standard requirement as the converter emits less conducted EMI. It gives even further miniaturization and reduces the production cost.

Most soft switching technique applied on PFC incorporates more than one active switch [5, 6, 7]. They also tends to only have ZVS characteristic. Therefore, this new active clamped-full wave-ZCS-boost topology provides improvement by providing ZCS-ZVS capability.
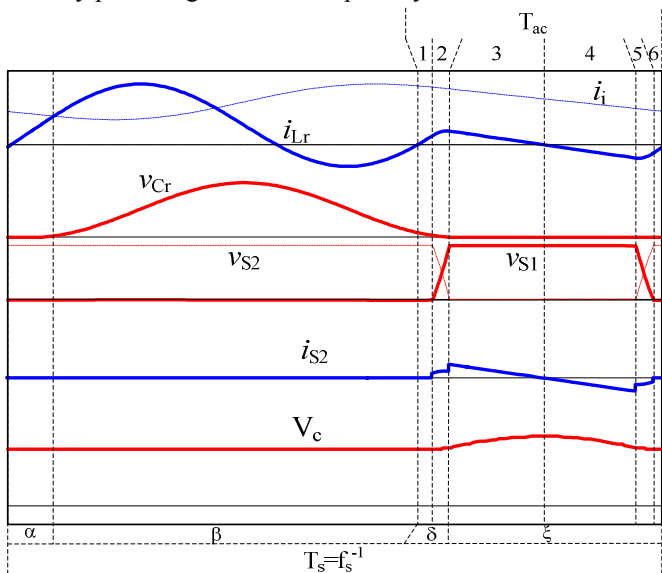

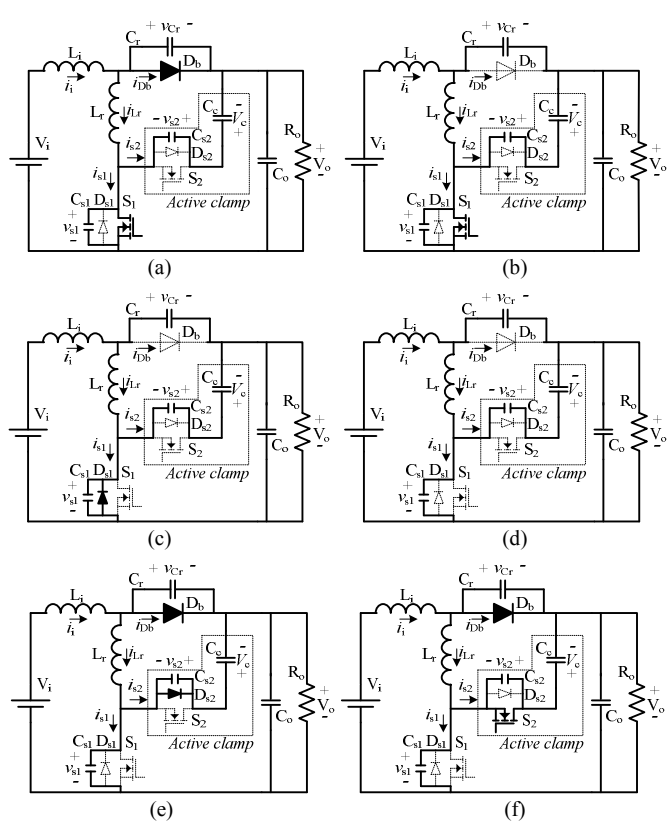Fig. 5. The active-clamped full-wave ZCS-QR boost converter operation stages

Fig. 6. Circuit operation stages of the proposed converter.

II. THE ACTIVE-CLAMPED SOLUTION

The proposed active-clamped full-wave ZCS-QR converter is shown on Fig. 4. (a). Impact of active-clamp technique application to the full-wave ZCS-QR boost converter key waveforms could be seen on Fig. 4. (b). It is shown there that no reverse recovery and abrupt current change can be found. It is also evident that S_1 experiences ZVS condition during its turn-on transition.

The active-clamped converter's operation stages could be analyzed from Fig. 5 and its corresponding circuit configurations shown on Fig. 6. (a) to (f). Generally, the involved process could be classified into two: (a) related to the ZCS-QR switch operation and (b) related to the active-clamp circuit.

The ZCS-QR Switch Operation Stages

Reference [8] gives detailed expression regarding full-wave ZCS-QR circuit operations. In that reference, all equations are normalized to resonant tank parameters:

$$f_0 = \frac{1}{2\pi\sqrt{L_r C_r}} = \frac{\omega_0}{2\pi} \tag{1}$$

$$\omega_0 t = \theta \tag{2}$$

$$R_0 = \sqrt{\frac{L_r}{C_r}} \tag{3}$$

$$J_s = I_i \frac{R_0}{V_o} \tag{4}$$

Basically, ZCS-QR switch operation is divided by four periods, those are α, β, δ, and ξ.

Up to the end of $\omega_0 t = \alpha$, circuit configuration on Fig. 7. (a) occurs. During this period, S_1 is turned on. It makes i_{s1} increase linearly. This circuit configuration ends when i_{s1} equals to i_i. Period of α could be determined by:

$$\alpha = J_s \tag{5}$$

The second period, β, is the resonant period. During this time, L_r and C_r are under resonant condition. Basically, this second period could be divided into positive and negative phase by considering phase of i_{Lr}. The positive phase of i_{Lr} corresponds to circuit on Fig. 6. (b). While the negative one corresponds to circuit on Fig. 6. (c). i_{Lr} equals to zero at the end of this period, that is when $\omega_0 t = \alpha + \beta$. For a full-wave topology, β can be found by:

$$\beta = 2\pi - \sin^{-1}(J_s) \tag{6}$$

The third period, δ, corresponds to circuit on Fig. 6. (d). During this time, v_{Cr} is discharged linearly up to zero. δ can be solved by applying equation (7) below,

$$\delta = \frac{1}{J_s}\left(1 + \sqrt{1 - J_s^2}\right) \tag{7}$$

The last period ξ is inserted in order to regulate average energy value processed by the ZCS-QR switch. The longer ξ, the smaller the processed average energy value.

From above explanations, one switching period consists of:

$$\omega_0 T_s = \alpha + \beta + \delta + \xi = 2\pi \frac{f_0}{f_s} = 2\pi \frac{1}{F_s} \tag{8}$$

Where, f_s is the switching frequency and F_s is

$$F_s = \frac{f_s}{f_0} \tag{9}$$

Maximum switching frequency is

$$\omega_0 T_s \geq \alpha + \beta + \delta = J_s + \left(2\pi - \sin^{-1}(J_s)\right) + \left(\frac{1}{J_s}\left(1 + \sqrt{1 - J_s^2}\right)\right) \tag{10}$$

Those timing considerations can be used to define a dimensionless variable μ as equivalent of duty cycle D that normally used in PWM converter. In order to define μ, it is important to determine the average value of i_{Lr}. Fig. 5 shows that the ZCS-QR switch process the energy only during α and β period. Therefore, the average value of i_{Lr} is defined as:

$$\langle i_{Lr}(t) \rangle_{T_s} = \frac{1}{T_s} \int_t^{t+T_s} i_{Lr}(t) dt = \frac{q_1 + q_2}{T_s} \tag{11}$$

Where q_1 is the energy processed on period α and q_2 on period β. From this, μ ideally will be:

$$\mu = \frac{\langle i_{Lr}(t) \rangle_{T_s}}{i_i} \approx F \tag{12}$$

As μ is a direct equivalent of D, boost converter steady state transfer function can be approximated by,

$$\frac{V_o}{V_i} = \frac{1}{1 - \mu} \tag{13}$$

The Active-Clamp Circuit Operation Stages

In an ideal circuit, current on S_1 ceased completely at the end of β. However, the real circuit realizes reverse recovery current

of D_{S1} and finite parasitic capacitance C_{s1}. Those two factors make i_{Lr} rises once more shortly after the end of β. This additional current makes energy storage on L_r not zero. Without any proper reset effort, this energy generates severe voltage ringing.

In the proposed topology, to alleviate voltage ringing problem, the end of β is the beginning of the active-clamp circuit operation. The active-clamp operation stages are explained as follows:

During period 1, i_{Lr} raise once more due to reverse-recovery charge q_{rr} of D_{S1}. This event stores energy as much as q_{rr} to L_r. During this period, circuit configuration is still depicted by Fig. 6. (c).

Period 1 over after all q_{rr} of D_{S1} being eliminated. It makes the beginning of period 2 where parasitic capacitance C_{s1} and C_{s2} is charged and discharged respectively. The circuit configuration changes to Fig. 6. (d). Charge and discharge currents occur under resonant condition of:

$$f_{01} = \frac{1}{2\pi\sqrt{L_r(C_{s1} + C_{s2})}} \tag{14}$$

$$R_{0_1} = \sqrt{\frac{L_r}{(C_{s1} + C_{s2})}} \tag{15}$$

Those occurrences make voltage on S_1 increase until reaching $V_o + V_c$ while voltage on S_2 decrease up to zero. It is important to note that this incident stores additional energy on L_r equal to:

$$q_{c_s} = (C_{s1} + C_{s2})(v_o + v_c) \tag{16}$$

After S_1 and S_2 reaches $V_o + V_c$ and zero respectively, period 2 over and period 3 started. During this period, energy stored on L_r is dumped to C_c through D_{s2} under resonant condition of:

$$f_{0c} = \frac{1}{2\pi\sqrt{L_r C_c}} \tag{17}$$

$$R_{0_c} = \sqrt{\frac{L_r}{C_c}} \tag{18}$$

During period 3, circuit configuration is indicated by Fig. 6. (e). To take advantages of ZVS condition, S_2 should be turned-on during this period. Circuit configuration changes to what is shown on Fig. 6. (f) when S_2 is turned-on.

After all energy on L_r dumped to C_c, the clamp current i_{s2} will be zero momentarily. This indicates the beginning of period 4. During this period, if S_2 is already turned on, i_{s2} will be flow in opposite direction towards L_r. This current returns under resonant condition like being stated in (17) and (18).

TABLE I
PARAMETERS LIST OF THE PROPOSED CONVERTER PROTOTYPE

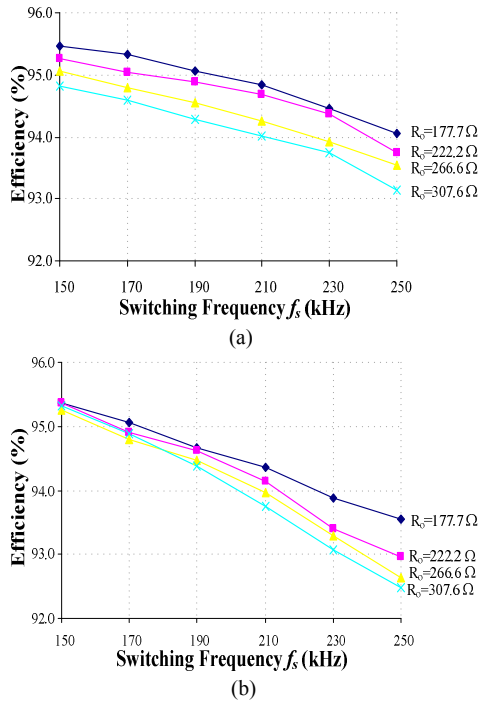| Resonant tank inductor	L_r	21 uH
Resonant tank capacitor	Cr	6.2 nF
Resonant tank frequency	f_0	441 kHz
Resonant tank impedance	R_0	58 Ω
Input inductor	L_i	220 uH
Output capacitor	C_o	330 uF
Clamp capacitor	C_c	520 nF
Input voltage	V_{in}	100 V

(a)

(b)

Fig. 7. Comparison of the converter efficiencies between (a) the active-clamped to (b) the diode-clamped full-wave ZCS-QR boosts converters.

At certain period before the beginning of the next switching cycle, S_2 should be turned off. This instance is the beginning of period 5. During this momment, charge on L_r discharges C_{s1} and charges C_{s2}. After all charges on those capacitors discharged and charged respectively, the remaining energy on L_r will flow through S_1 body diode to C_o. It is evident here that S_1 experiences ZVS transition during next switching cycle as the C_{s1} is already discharged at the beginning of the next switching cycle.

Influence of The Active-Clamp Circuit to μ

The average value of i_{Lr} on Fig. 5 during active-clamped period (T_{ac}) can be found by:

$$\langle i_{Lr}(t)\rangle_{T_{ac}} = \frac{1}{T_{ac}}\int_0^{T_{ac}} i_{Lr}(t)dt = 0 \qquad (19)$$

That was because

$$\langle i_{Lr}(t)\rangle_{T_{ac1}+T_{ac2}+T_{ac3}} = -\langle i_{Lr}(t)\rangle_{T_{ac4}+T_{ac5}+T_{ac6}} \qquad (20)$$

Therefore, it can be concluded here that the active-clamp circuit do not have any influence on μ. Therefore, equation (12) and (13) is still valid in order to calculate ideal steady state transfer function of the proposed boost converter.
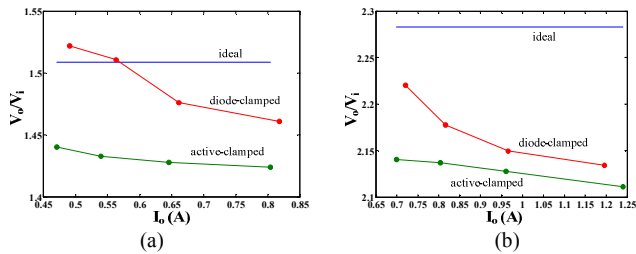

Fig. 8. The converter's voltage regulation characteristic under (a) 150 kHz and (b) 250 kHz for various loads current
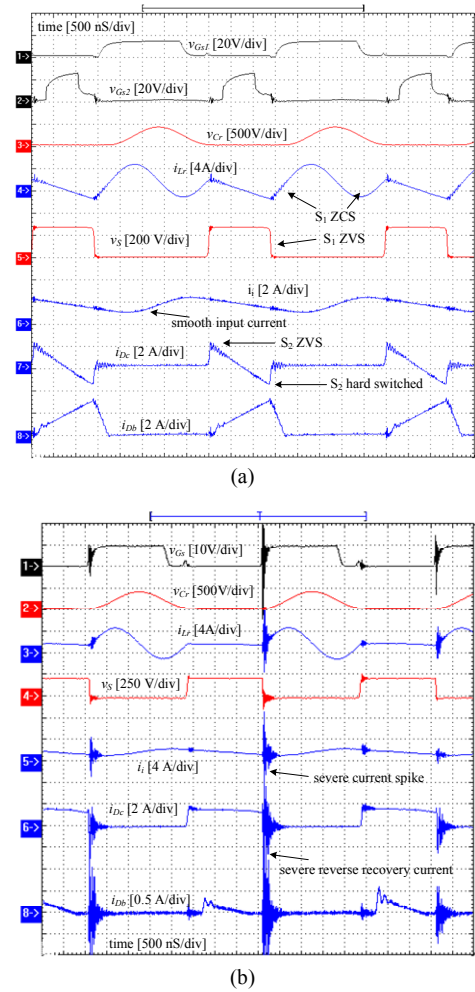

(a)

(b)

Fig. 9. Key waveforms comparison between (a) the active-clamped to (b) the diode-clamped full-wave ZCS-QR boost converter.

III. EXPERIMENTAL RESULT

Two prototypes with almost identical key parameters have been built to confirm the aforementioned hypothesis. The first prototype is based on diode-clamped topology, while the other one is the active-clamped topology. The specification of key parameters for both converters is listed in Table 1.

Efficiency Comparison

Fig. 7 shows the efficiency comparison of the active-clamped topology to the former diode-clamped topology. It can be seen that even though the peak efficiency among them are quite similar (95.6%) but the proposed topology gives more uniform performance under given operating frequency (150 - 250 kHz) and load range.

It should be pointed out that converter's efficiency at high frequency is better compared to former converter. This higher efficiency is the result of the ZVS condition during S_1 turn-on. With ZVS transition, less energy losses due to parasitic capacitance occurs. This capacitance loss it the main source of inefficiency during high-frequency operation [8].
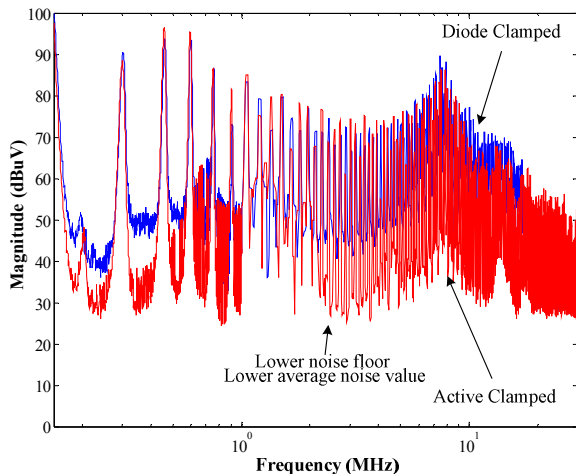
Fig. 10. Conducted EMI characteristics of the proposed converter

However, the proposed converter efficiency under low-frequency and lightly-loaded condition is slightly deteriorated. This is because the active-clamped circuitry provides more parasitic burden compared to the simpler diode-clamped solution stated on [3]. In this operating condition, the advantage of ZVS transition to converter's efficiency is less obvious.

Voltage Regulation Characteristics

It is important to know about the voltage regulation characteristics of the proposed converter. Fig. 8 depicted that the proposed topology gives better voltage regulation performance compared to former diode-clamped solution. It can be seen that V_o of the proposed converter only changes in narrow range even I_o changes for almost 1 to 2 ratio. However, this figure also indicates that the proposed converter gives more deviation to ideal output voltage (V_o).

The real experimental results of the key waveforms are presented on Fig. 9. It is evident that the active-clamped topology gives superior performance to the diode-clamped one in term of waveform transition smoothness. Figures show that the input current i_i of the proposed converter is cleaner compared to the previous converter. There are also no significant oscillations can be found. Also, it has less abrupt changes to be occurred on its voltages and currents waveforms. These better waveforms characteristics are due to less reverse recovery diode problem and ZVS switching action of S_1 during its turn-on transition.

Conducted EMI Measurement

It is also interested to see the effect of smoother key waveforms of the proposed converter in relation to its conducted EMI characteristics. To reveal that, some EMI measurements have been done by using rohde-schwarz LISN ESH2-Z5. During test, both converters were operated with 100 V_{in}, 330 Ω R_o, 150 kHz operating frequency, and without any EMI input filters attached to it. The EMI measurement result can be seen on Fig. 10.

From the figure it is revealed that the proposed boost converter gives lower conducted noise floor. This character contributes towards lower average conducted noise energy. Other than that, at some points, the proposed boost converter also provides lower peak EMI value. Those good points may relax the effort of conduction noise filtering.

IV. CONCLUSIONS

A topology called active-clamped full-wave zero-current-switched quasi-resonant boost converters has been demonstrated. Its basic operation principles, involved equations, and experimental results have been presented. This new topology has proven to be able to alleviate the voltage ringing phenomena during switch turn-off period on a full-wave ZCS-QR boost converter. Beside that, active clamp circuit also gives additional benefit by adding ZVS characteristic to current converter. It has been shown that this technique performance is better if compared to former simple diode clamp topology in terms of efficiency, voltage regulation, and conducted EMI characteristics. This topology offers good candidate in a boost power factor correction application.

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