A Power Efficiency Improvement Technique for A Bi-Directional Dual Active Bridge DC-DC Converter at light load

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***Abstract*— Recently, the bi-directional dc-dc converter has been focused on because of the huge demand for diversification of power supply network including battery. The dual active bridge (DAB) dc-dc converter is one of the most popular circuits for bi-directional applications because of its simple structure. However, power efficiency at light load is the intrinsic problem of a bi-directional DAB DC-DC converter. In this paper, the simple solution with digital operation for the problem is proposed and experiments are performed with 1kW system. This method can reduce a switching surge without other circuits such as snubber and improve power efficiency at light load. Therefore it can reduce loss of switching surge and, improve power efficiency. From the results, 37% maximum power efficiency improvement at light load is confirmed. Furthermore, this method is capable of control in the conventional method in the heavy load range. Consequently, it is possible to reduce the switching surge and realize high power efficiency in a wide load range.**

I. INTRODUCTION

Recently, the bi-directional dc-dc converter has been focused on because of the huge demand for diversification of power supply network including battery. The DAB dc-dc converter is one of the most popular circuits for bi-directional applications because of its simple structure [1-6]. However, a switching surge and power efficiency at light load condition is the intrinsic problem [4].

Some research have been done to solve the problem, for instance, use of resonant type converter with snubber circuit [1], silicon carbide (SiC) power device and new magnetic materials [2], Quasi-ZCS operation with LC filter [3], and converter linked through superposition in additive polarity in series[4].

This paper proposes a simple solution for power efficiency improvement with digital operation. This method can improve power efficiency due to reduce a switching loss without adding other circuits such as snubber.

II. CONVENTIONAL OPERATION OF A DAB DC-DC CONVERTER

Fig. 1 shows the circuit schematic of the basic DAB dc-dc converter. Fig. 2 shows the operating waveforms with the conventional operation [5]. In the conventional operation, the output power is operated by the phase-shift shown as φ between the primary voltage v_P and secondary voltage v_S of transformer. Fig. 3 shows the phasor diagram. V_P, V_S, V_L, and I are phasor symbols for v_P, v_S, v_L, i, respectively. When

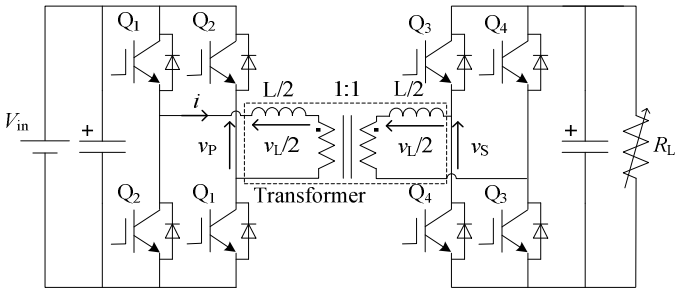
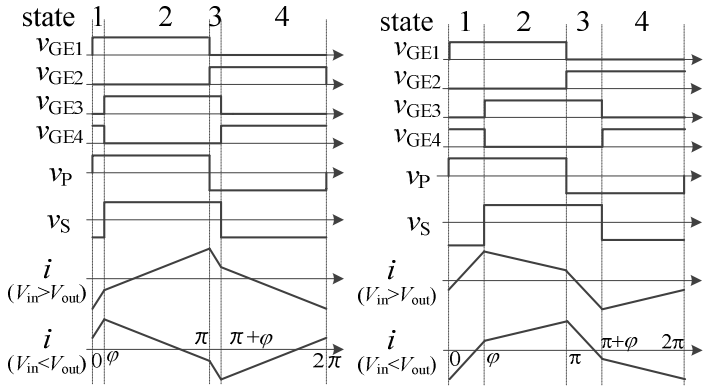


Figure 1. The circuit schematic of DAB dc-dc converter.



(a) (b)

Figure 2. Conventional operating waveform: (a) light load; (b) heavy load.

V_S is lagging V_P in power running mode (Fig. 3 (a) and (b)), and when V_S is leading V_P, it is operated in power regenerative mode (Fig. 3 (c)).

The output power P_o can be obtained as

$$P_o = \frac{V_{in}V_{out}}{\omega L}\varphi(1-\frac{\varphi}{\pi}). \quad (1)$$

The output power can be controlled with the phase difference φ. The waveform of the current i is changed by the load condition. In this paper, current i crossed the zero line in the state 2 is defined as a light load, and current i crossed the zero line in the state 1 is defined as a heavy load as shown in Fig. 2.

III. Intrinsic Surge Problem Of A DAB Dc-dc Converter

Well known problem of a DAB DC-DC converter is switching surge in the light condition. It is caused by the reverse recovery effect of the diode. Fig. 4 shows φ - P_o. The switching surge occurs at hard switching range of this figure.

Fig. 5 shows the generation mechanism of switching surge when $V_{in} > V_{out}$. The surge voltage occurs in the transition from state 1 (3) to state 2 (4), repeatedly. C_d is the parasitic capacitance of diode which is connected in parallel with the ideal diode, and L_{wire} is parasitic reactance. At the light load condition, the diodes D_4 is conducting in state 1. Then the switches Q_3 is turned on when state changes from state 1 to state 2. At this instantaneous moment, the

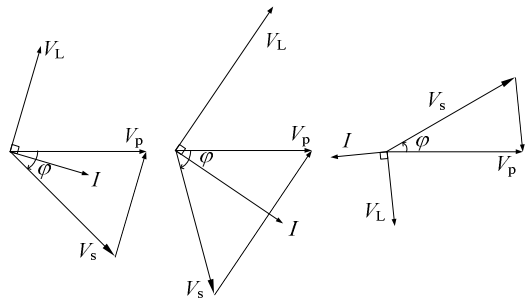


Figure 3. Phasor diagram[1]: (a) power running mode (light load); (b) power running mode (heavy load); (c) power regenerative mode.

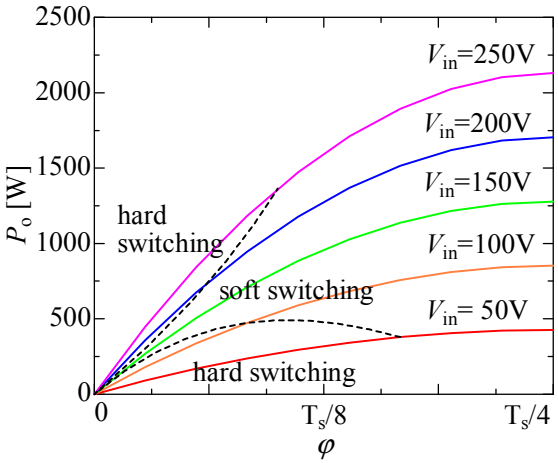
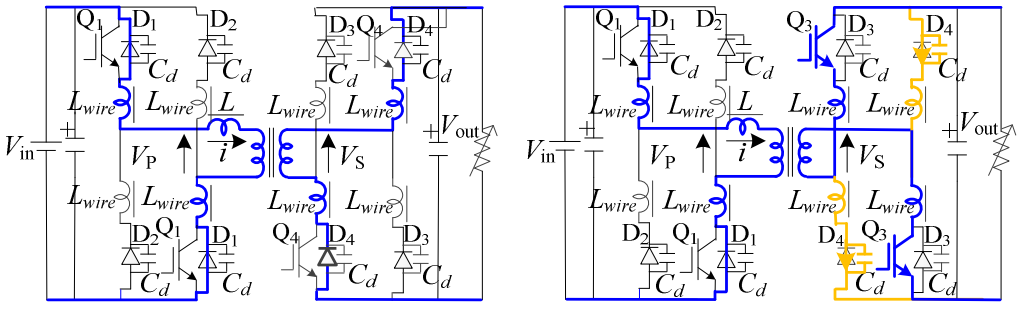


Figure 4. φ - *P*o [1].

diode D_4 is switched from a forward bias condition to a reverse bias condition immediately. And the switching surge is occurred with the resonance of C_d and L_{wire} due to reverse recovery phenomenon. With the same reason, when $V_{in} < V_{out}$, the surge occurs in the transition from state 2 (4) to state 3 (1) on the primary side.

Commonly, to protect the switches from the switching surge, snubber circuit are applied [2]. However, the power loss at the snubber circuit can't be ignored at the light load condition. The other way, the resonant converter type is also popular, but the additional components are needed.



(a) state 1 (b) state 2

Figure 5. The generation mechanism of switching surge.

IV. Proposed Operation Method

We have proposed the software-based compensation method for basic DAB bi-directional dc-dc converter which can be reduce the switching surge at the light load, without any of additional circuits such as the snubber circuits or resonant circuits [7]. Fig. 6 shows idealized waveform of the proposed operating method. With this method, it can easily change alternately buck mode and boost mode operation. When $V_{in} < V_{out}$, as it can be seen from the waveforms, the direction of primary side current of transformer i during each on-time of Q_1 and Q_2, is restricted to avoid the crossing the zero line. Due to the restriction of the change of the direction of the current, the zero-current-switching-on can be realized for Q_1 and Q_2. The ideal analysis has been done for each of buck mode and boost mode operation, respectively. This converter has six operational states in one switching period for each of the buck and boost mode operation, respectively. The elements are treated as ideal in equivalent circuit.

The detailed description of the ideal circuit is revealed in a previous paper [7]. Therefore, only the results are shown in this paper.

A. Buck Mode Operation in light load

In buck mode, the primary side switches Q_1 and Q_2 are turned-on twice in the period. Firstly, Q_1 and Q_2 are turn-on at $t = 0$ and $T_s / 2$. Secondly, they are turn-off at $t = A$ and $T_s / 2 + A$. Thirdly, they are turn-on at $t = \varphi$ and $T_s / 2 + \varphi$. Fourthly, they are turn-off at $t = T_s / 2$ and T_s.

A is calculated as

$$A = \frac{V_i - V_o}{V_i + V_o}\left(\frac{1}{2}T_s - \varphi\right). \tag{2}$$

B. Boost Mode Operation in light load

In boost mode, the secondary side switches Q_3 and Q_4 are turned-on twice in the period. Firstly, Q_3 and Q_4 are turn-on at $t = \varphi$ and $T_s / 2 + \varphi$, respectively. Secondly, they are turn-off at $t = B$ and $T_s / 2 + B$. Thirdly, they are turn-on at $t = T_s / 2$ and 0. Fourthly, they are turn-off at $t = T_s / 2 + \varphi$ and B.

B is calculated as

$$B = \frac{2V_o}{V_o - V_i}\varphi. \tag{3}$$

C. Output power control in light load

The ideal analysis for both of buck and boost mode operation can be done in uniformly. For the ideal analysis result, the output power P_o can be obtained as

$$P_o = \frac{2X^2}{T_s L}\cdot\left|\frac{V_i + V_o}{V_i - V_o}\right|\cdot V_i V_o. \tag{4}$$

In buck mode, $X = A$, and in boost mode, $X = \varphi$.

D. Output Power control in heavy load

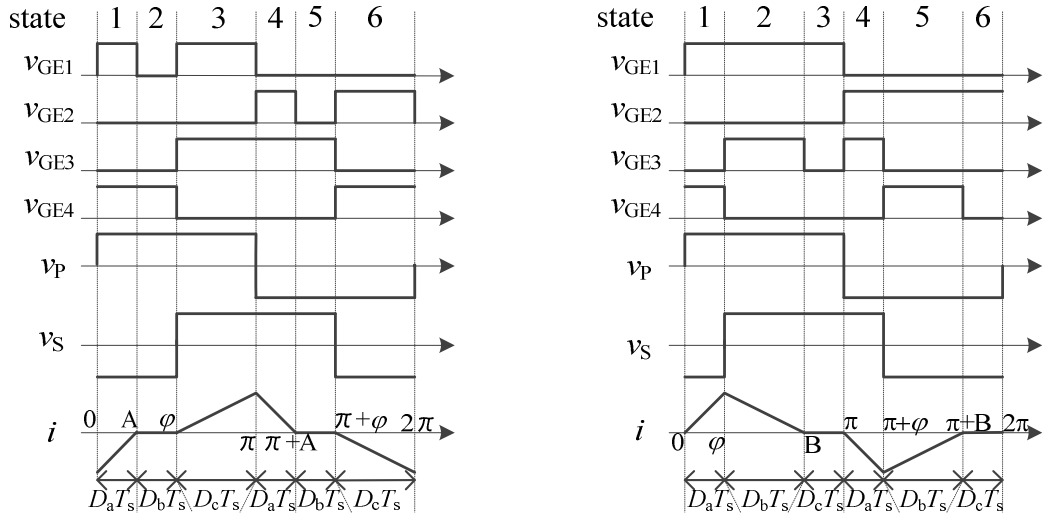
In the light load, with the output power increasing, the periods of which all switches turned OFF ($A \sim \varphi$, $\pi+A \sim \pi+\varphi$, $B \sim \pi$, $\pi+B \sim 2\pi$) becomes shorter. The periods, equal to zero seconds, it is the boundary between light load and heavy load. Therefore, in the heavy load condition, the only conventional phase-shift operation is active. From the results, it can be seen that it is possible to control the output power seamlessly despite of the load condition. Relationship φ and P_o of conventional and proposed operation is shown in Fig. 7.

E. Pulse generating method

Fig. 8 and Fig. 9 show the generating mechanism of proposed drive signal. As mentioned above, the gate signal is the combination of the phase shift signal and the masked signal. The mask width is calculated and controlled by Eq. (2) and (3), respectively.

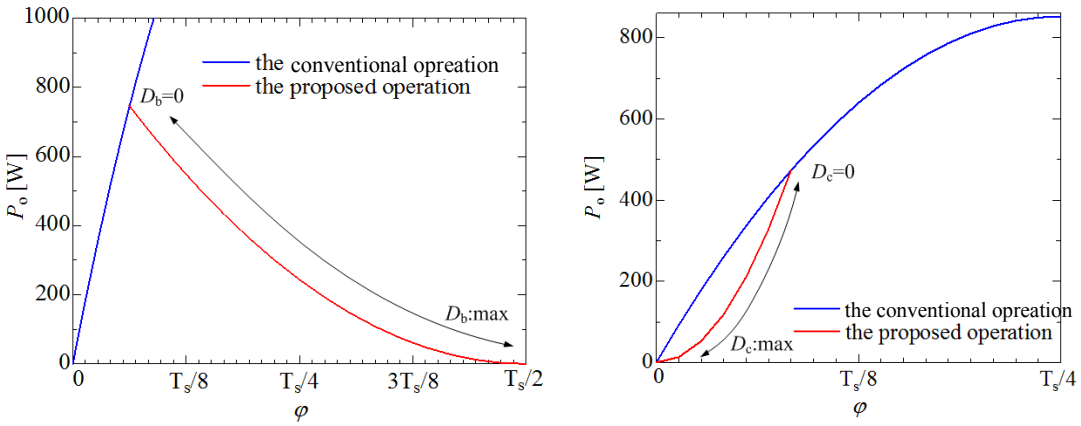
V. Loss Included analysis Of conventional Operation

The loss included analysis of conventional operation is shown in a previous paper [8]. Therefore, only the results are



(a) buck mode (b) boost mode

Figure 6. Idealized wave form for proposed operating at the light load: (a) buck mode; (b) boost mode.



(a) buck mode (b) boost mode

Figure 7. φ - *Po* (conventional operation and proposed operation).

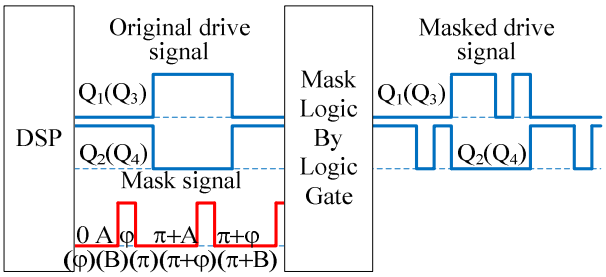


Figure 8. Masked drive signal generating mechanism.

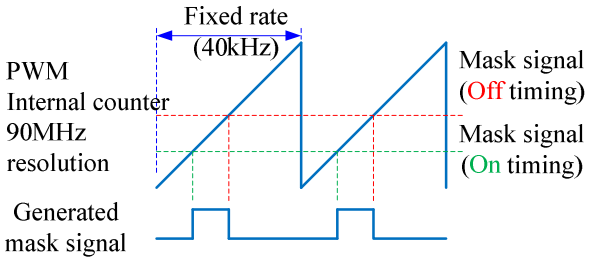


Figure 9. Mask signal generating mechanism by PWM peripheral in DSP.

shown in this paper. Output power including the loss is

$$P_o = \frac{V_{in}V_{out}}{2}\varphi\left(1-\frac{\varphi}{\pi}\right)\left[\frac{V_o/V_i+1}{\omega L+r_{loss}\varphi}-\frac{V_o/V_i-1}{\omega L+r_{loss}(\pi-\varphi)}\right]. \quad (5)$$

VI. Loss Included Analysis Of Proposed Operation

To analyze the characteristics of the circuit, Extended State-Space Averaging Method [9] is applied. The analysis has been done for each of buck mode and boost mode operation, respectively. In order to simplify the loss analysis, loss is defined as r_{loss}.

A. Buck Mode Operation

Equivalent circuits corresponding to each state in buck mode operation are shown in Fig. 10, where $\hat{v}_o$ is the low-frequency component of V_o. $D_a = A - 0$, $D_b = \varphi - A$, $D_c = \pi - \varphi$ in Fig. 6 (a). For ease of analysis, the calculation has been performed in a half of the switching period because of the symmetric behavior of the circuit.

For analysis, solving for i_L and i_c,

for $0 \le t \le A$ (state 1)

$$i_L = \frac{(V_i+\hat{v}_0)t}{L+r_{loss}t}+\frac{L}{L+r_{loss}t}i(0) \quad (6)$$

$$i_C = -i_L - \frac{\hat{v}_o}{R_L} \quad (7)$$

for $A \le t \le \varphi$ (state 2)

$$i_L = 0 \quad (8)$$

$$i_C = -i_L - \frac{\hat{v}_o}{R_L} \quad (9)$$

for $\varphi \le t \le \pi$ (state 3)

$$i_L = \frac{(V_i-\hat{v}_0)\{t-(D_a+D_b)T_s\}}{L+r_{loss}\{t-(D_a+D_b)T_s\}} \quad (10)$$

$$i_C = i_L - \frac{\hat{v}_o}{R_L}. \quad (11)$$

From Fig. 6, it is clear that $D_a + D_b + D_c = 1/2$, $i_L(0) = -i_L(\pi)$ and $i_L(A) = 0$. Using the preceding relationships,

$$i_L(0) = -i_L(\pi) = -\frac{(V_i+\hat{v}_0)D_aT_s}{L} \quad (12)$$

and

$$D_c = \frac{V_i+\hat{v}_o}{V_i-\hat{v}_o-2D_aT_s\hat{v}_or_{loss}/L}D_a. \quad (13)$$

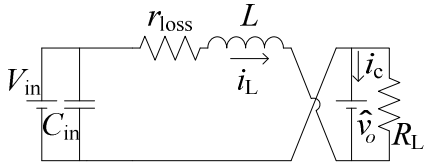
The average value of v in each state is calculated with

$$i_{c\_ave1} = -\frac{1}{2}\frac{(V_i+\hat{v}_0)D_aT_s}{L}-\frac{\hat{v}_o}{R_L} \quad (14)$$

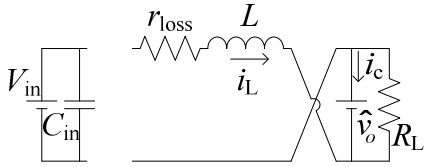
$$i_{c\_ave2} = -\frac{\hat{v}_o}{R_L} \quad (15)$$

$$i_{c\_ave3} = -\frac{1}{2}\frac{(V_i+\hat{v}_0)D_aT_s}{L}-\frac{\hat{v}_o}{R_L}. \quad (16)$$

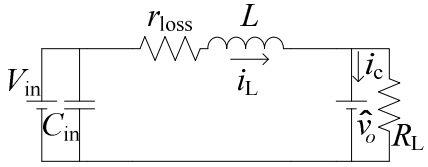
Hence,



(a) state 1

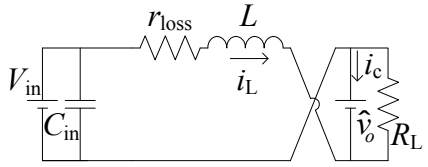


(b) state 2

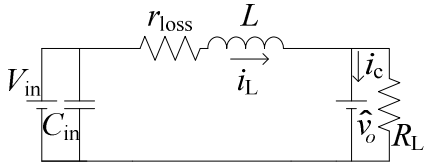


(c) state 3

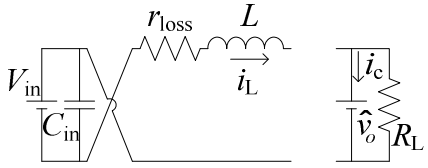
Figure 10. Equivalent circuit of buck mode operation: (a) state 1; (b) state 2; (c) state 3.



(a) state 1



(b) state 2



(c) state 3

Figure 11. Equivalent circuit of boost mode operation: (a) state 1; (b) state 2; (c) state 3.

$$\overline{i_c} = 2(i_{c\_ave1} \times D_a + i_{c\_ave2} \times D_b + i_{c\_ave3} \times D_c) = \frac{2D_a^2 T_s}{L} \cdot \frac{(V_i + \hat{v}_o)(V_i - \hat{v}_o D_a T_s r_{loss} / L)}{(V_i - \hat{v}_o)} - \frac{\hat{v}_o}{R_L}. \quad (17)$$

The results of static characteristics are obtained by letting $d\hat{v}_o / dt = 0$, therefore

$$\overline{i_c} = C\frac{d\hat{v}_o}{dt} = 0 \quad (18)$$

$$P_o = \frac{2D_a^2 T_s}{L} \cdot \frac{(V_i + V_o)(V_i V_o - V_o{}^2 D_a T_s r_{loss} / L)}{(V_i - V_o)}. \quad (19)$$

Using $D_a T_s = A$,

$$P_o = \frac{2A^2}{T_s L} \cdot \frac{(V_i + V_o)(V_i V_o - V_o{}^2 D_a T_s r_{loss} / L)}{(V_i - V_o)} \quad (20)$$

where

$$A = \frac{(V_i - V_o)(T_s / 2 - \varphi)}{V_i + V_o + 2V_o(T_s / 2 - \varphi) r_{loss} / L}. \quad (21)$$

B. Boost Mode Operation

Equivalent circuits corresponding to each state in boost mode operation are shown in Fig. 11 For analysis, equation is formularized for each state. $D_a = \varphi - 0$, $D_b = B - \varphi$, $D_c = \pi - B$ in Fig. 6 (b).

For $0 \le t \le \varphi$ (state 1)

$$i_L = \frac{(V_i + \hat{v}_0)t}{L + r_{loss} t} \quad (22)$$

$$i_C = -i_L - \frac{\hat{v}_o}{R_L} \quad (23)$$

for $\varphi \le t \le B$ (state 2)

$$i_L = \frac{(V_i - \hat{v}_0)(t - D_a T_s)}{L + r_{loss}(t - D_a T_s)} + \frac{L}{L + r_{loss}(t - D_1 T_s)} i(D_a T_s) \quad (24)$$

$$i_C = i_L - \frac{\hat{v}_o}{R_L} \quad (25)$$

for $B \le t \le \pi$ (state 3)

$$i_L = 0 \quad (26)$$

$$i_C = -\frac{\hat{v}_o}{R_L}. \quad (27)$$

From Fig. 6, it is clear that $D_a + D_b + D_c = 1/2$, and $i_L(B) = 0$. Using the preceding relationships

$$D_b = -\frac{(V_i + \hat{v}_o)}{(V_i - \hat{v}_o)(1 + D_a T_s r_{loss} / L)} D_a. \quad (28)$$

Hence,

$$\overline{i_c} = -\frac{2D_a^2 T_s}{L} \cdot \frac{(V_i + \hat{v}_o)}{(V_i - \hat{v}_o)} \cdot \frac{\{V_i + (V_i - \hat{v}_o) D_a T_s r_{loss} / 2L\}}{(1 + D_a T_s r_{loss} / L)^2} - \frac{\hat{v}_o}{R_L}. \quad (29)$$

The results of static characteristics are obtained by letting $d\hat{v}_o / dt = 0$, therefore

$$P_o = \frac{2(D_a T_s)^2}{T_s L} \cdot \frac{(V_i + V_o)}{(V_i - V_o)} \cdot \frac{\{V_i V_o + V_o(V_i - V_o) D_a T_s r_{loss} / 2L\}}{(1 + D_a T_s r_{loss} / L)^2}. \quad (30)$$

Using $D_a T_s = \varphi$

$$P_o = \frac{2\varphi^2}{T_s L} \cdot \frac{(V_i + V_o)}{(V_i - V_o)} \cdot \frac{\{V_i V_o + V_o(V_i - V_o)\varphi\, r_{loss} / 2L\}}{(1 + \varphi\, r_{loss} / L)^2}. \quad (31)$$

B is calculated as

$$B = (D_a + D_b)T_s = \frac{-2V_o - (V_i - V_o)\varphi\, r_{loss}/L}{(V_i - V_o)(1 + D_a T_s r_{loss}/L)}\varphi. \quad (32)$$

VII. Experimental Results

In order to select the value of r_{loss}, we perform some experiments with the prototype circuit. The main circuit is DAB dc-dc converter without additional circuits like snubber circuit. We had closed loop operation experiments with DSP TI TMS320F28335. Experimental parameters are shown in Table I. Dead time of each switch is 1μs.

A. Surge Reduction

Fig. 12 shows the waveform of the corrector-emitter voltage and the corrector current of the low voltage side bridge of the buck converter. Fig. 12(a) shows the result of the conventional operation and Fig. 12(b) shows the result of the proposed operation. Comparing with these results, it can be seen that 99% of voltage surges and 100% of current serge of reduction.

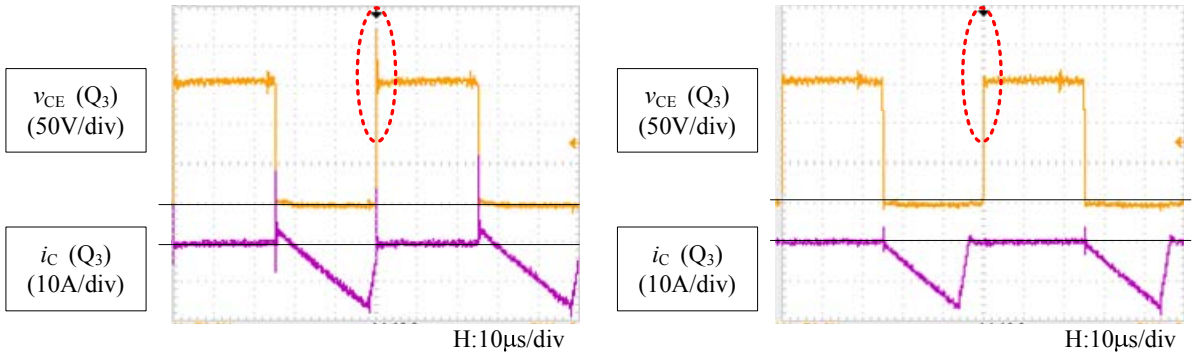
Fig. 13 shows the waveform of the boost converter. Comparing with these results, it can be seen that 99% of voltage surges of reduction and 100% of current serge of reduction.

B. Power efficiency

Fig. 14 and Fig. 15 show the comparison of the current waveforms of i_L in the condition of the regulated output voltage. From the results, it can be seen that the amount of the i_L

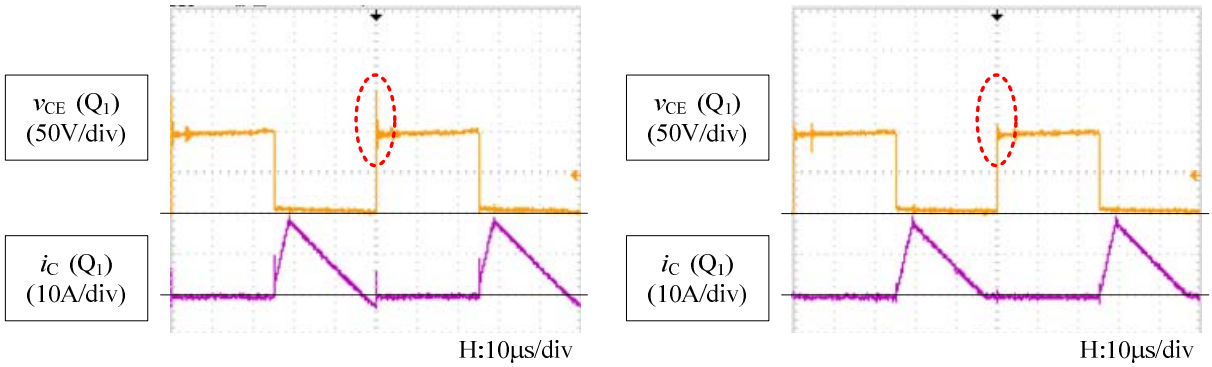
TABLE I. Specification of DAB DC-DC converter

Item	*Symbol*	*Specification*
Transformer		
1) Turns ratio	A	1:1
2) Leakage inductance(primary-referred)	L	110μH
Converter		
1) Rated output power	P_o	1kW
2) Rated input direct voltage	V_{in}	150V
3) Rated output direct voltage	V_{out}	150V
4) Switching frequency	f_s	20kHz
5) Absolute maximum ratings of IGBT collector-emitter	v_{CE}	600V
6) On resistance of IGBT	r_t	50mΩ
7) Absolute maximum ratings of diode	i_F	30A
8) Forward voltage of diode	v_F	0.8V
9) Recovery time of diode	t_{rr}	0.1μs



(a) the conventional operation (b) the proposed operation

Figure 12. The waveforms in buck mode: (a) the conventional operation (V_{in}=200V, V_{out}=150V, P_o=504W); (b) the proposed operation. (V_{in}=200V, V_{out}=150V, P_o=502W)



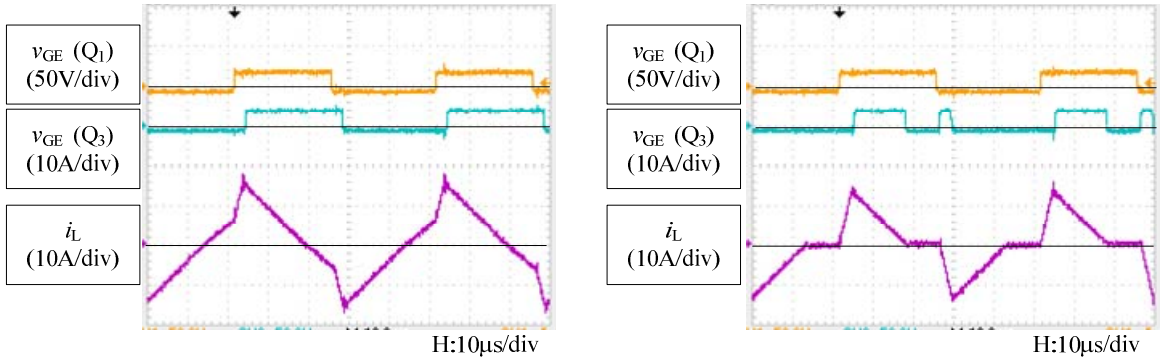
(a) the conventional operation (b) the proposed operation

Figure 13. The waveforms in boost mode: (a) the conventional operation (V_{in}=100V, V_{out}=150V, P_o=687W); (b) the proposed operation. (V_{in}=100V, V_{out}=150V, P_o=686W)

of the can be decreased with the proposed operation. With these results, the ohmic loss at the parasitic resistor is also decreased. Fig. 16 shows the power efficiency results for the both of the conventional and the proposed operation. It can be seen that the power efficiency of buck mode can be apparently improved by up to 37% using the proposed operation at 100W as shown in Fig. 16 (a). It can be seen that the power efficiency of boost mode can be apparently improved by up to 30% at 100W as shown in Fig. 16 (b).

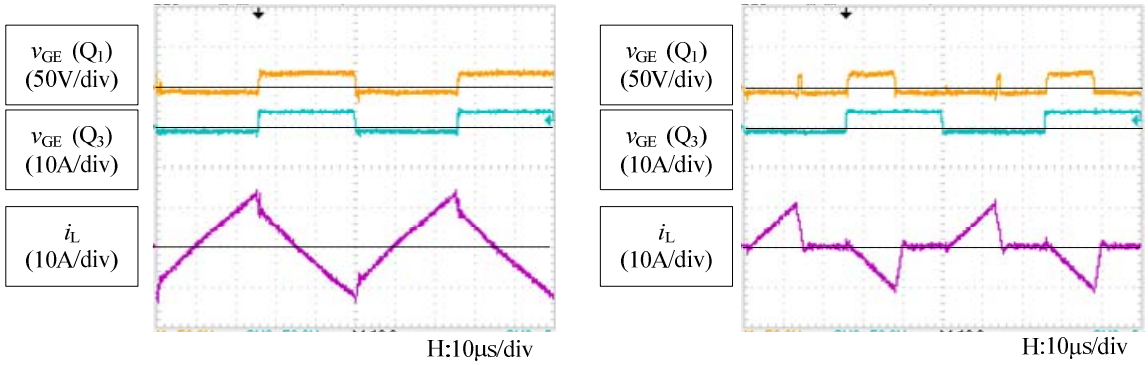
C. *Estimating the Value of Loss*

Fig. 17 shows φ - P_o of analysis and experimental results. For the analysis, r_{loss} is estimated. r_{loss} is set 1.5Ω for the conventional operation and r_{loss} is set 0.5Ω for the proposed operation. This difference of r_{loss} is due to the differences of the current path. Using these r_{loss} values for both of them, differences between loss including analysis and experimental results are 10% or less in more than 100W. In less than 100W, error is greater than 10% because of measuring preci-



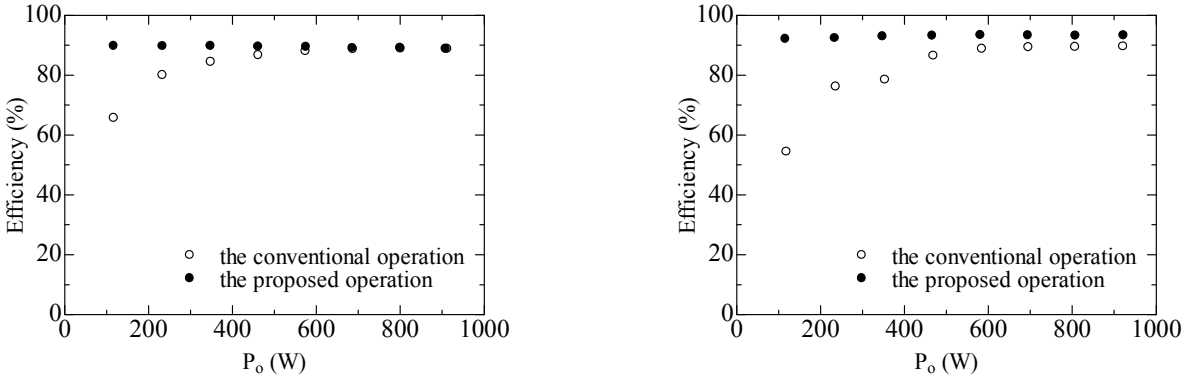
(a) the conventional operation (b) the proposed operation

Figure 14. The comparison of the current waveforms of i_L: (a) the conventional operation (V_{in}=100V, V_{out}=150V, P_o=200W); (b) the proposed operation (V_{in}=100V, V_{out}=150V, P_o=200W).



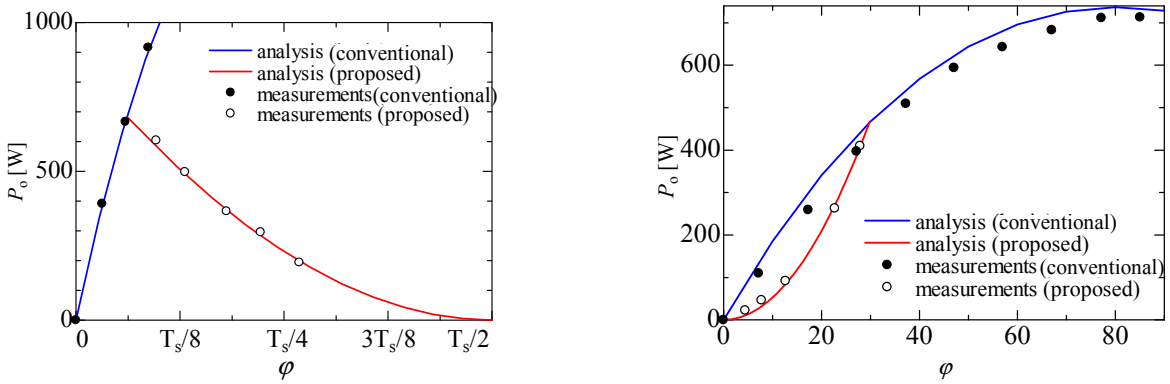
(a) the conventional operation (b) the proposed operation

Figure 15. The comparison of the current waveforms of i_L: (a)the conventional operation (V_{in}=200V, V_{out}=150V, P_o=200W); (b) the proposed operation (V_{in}=200V, V_{out}=150V, P_o=191W).



(a) buck mode (b) boost mode

Figure 16. Power efficiency: (a) buck mode (V_{in}=200V, V_{out}=150V); (b) boost mode (V_{in}=100V, V_{out}=150V).



(a) buck mode (b) boost mode

Figure 17. φ - P_o (analysis and experimental results).

sion. The results revealed that the analysis can be used to design the circuit.

D. Compensation for floating terminalof transformer

There is a state that the terminal of the transformer is open in the proposed operation. As the control option, it is possible to avoid the opening of the transformer by reducing the OFF time (A ~ φ, B ~ π). One of the examples is shown in Fig. 18.

VIII. CONCLUSION

By the analysis of the circuit operation and the some experiments, the validation of the proposed operation for DAB dc-to-dc converter is revealed. Applying the two modes which are proposed operation in light load and conventional operation in heavy load, the circuit can be operated in the full load range. The operation method with digital operation can reduce switching surges without other circuits like snubber circuit. From the experiment results, the 99% of the maximum voltage surge reduction and 100% of the maximum current serge reduction at the light load is confirmed. Furthermore, due to the surge reduction method, 37% maximum power efficiency improvement can be confirmed at light load.

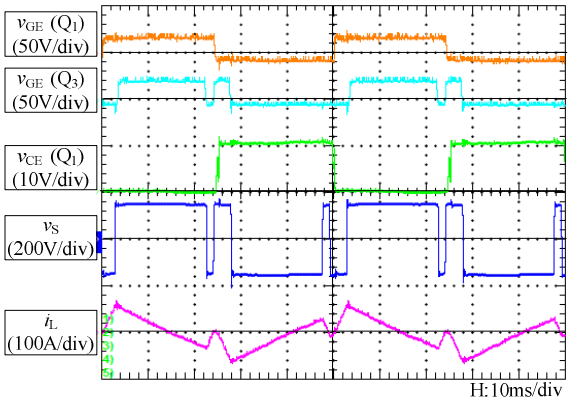


Figure 18. operation by reducing the OFF time. (V_{in}=100V, V_{out}=150V, P_o=200W)

Furthermore P_o can be assumed with loss included analysis. Using r_{loss} = 1.5Ω at conventional operation and r_{loss} = 0.5Ω at proposed operation, differences between loss including analysis and experimental results are 10% or less in more than 100W.

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