5MHz PWM-Controlled Current-Mode Resonant DC-DC Converter with GaN-FETs

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***Abstract*— In this paper, a proposed pulse width modulation (PWM) control method for the isolated current-mode resonant DC-DC converter with MHz level switching frequency is presented. The circuit topology is same as a conventional resonant converter with synchronous rectification and without any additional components. The control technique for the output voltage regulation is proposed with the unique PWM control for synchronously-rectifying switches. By using the transformer's leakage inductance and the PWM control, the boost conversion can be realized. In addition, to achieve the zero-voltage switching (ZVS) operation, phase-shift between primary and secondary-side switches is adapted. The ZVS operation can maintain for primary-side switches. In this paper, proposed technique for achieving stable ZVS operation has been discussed. Some experiments have been done with 5MHz isolated DC-DC converter which has Gallium Nitride field effect transistor (GaN-FET), and the total volume of the circuit is 16.14cm^3. The data show that the maximum power efficiency is 89.4%.**

I. INTRODUCTION

Recently, high power-efficiency and high power-density DC-DC converters have been required in a wide field of applications. Corresponding to this requirement, the current-mode resonant DC-DC converters featuring high power-efficiency have been continuously developed. Furthermore, the increase in the switching frequency of these converters is considered to be one of key technologies needed for down-sizing. We have also developed a 5MHz current-mode resonant DC-DC converter, and presented its prominent features previously [1]. The converter had an input/output voltage of 48V/12V and a power rating of 120W. In this converter, GaN-FETs were utilized as semiconductor switches, which were suitable for high-frequency switching operation. Also, another researches have been proved utilizing GaN-FET for high frequency converter is very practical [2-9].

Current-mode resonant DC-DC converters are usually controlled by pulse frequency modulation (PFM). However, PFM control is hard to design to control the output voltage at MHz level switching frequency operation. The detail is described later.

To solve the issue, this paper presents a new PWM control method for the current-mode resonant converter with MHz level switching frequency. This converter topology is same as the conventional current-mode resonant converter with synchronous rectification. The feature of the converter is controlling the output voltage without any additional components. By using transformer's leakage inductance and secondary-side synchronously rectifying switches, the new control method for boost conversion is realized.

In the previous researches, some PWM-controlled current-mode resonant DC-DC converters have been presented [10-15]. The most recent PWM-controlled resonant converters utilized the control technique for duty ratio of primary-side switches, and some additional components such as an active clamp switch or output inductance were needed. On the other hand, the advantages of the proposed converter are controlling secondary-side switches and no additional components.

However, the proposed converter cannot be achieved ZVS operation with the conventional method which uses magnetizing current. Therefore, to accomplish the ZVS operation in the proposed converter, phase-shift between primary and secondary-side switches which control resonant current is adapted. As a result, this proposed converter maintains some fundamental characteristics of resonant operation such as ZVS of main switches.

In this paper, the novel PWM control method for the current-mode resonant converter with MHz level switching frequency is proposed. In the section II, the issue of the conventional current-mode resonant converter in MHz level operation is described. In the section III, the principle of the proposed control technique and the ZVS operation technique is revealed. In the section IV, some experimental results have confirmed the capability of output-voltage control and ZVS operation with the 5MHz resonant converter using GaN-FET.

II. The Issue of The Conventional Current-Mode Resonant Converter Control in MHz Level Operation

Recently, for DC-DC converters, high power-density and high power-efficiency are strongly demanded. To realize the high power-density, operating DC-DC converter in the high frequency is valid because of the minimizing the value of the magnetic transformer. However, with the high frequency switching, switching loss is becoming larger. To suppress the switching loss, the current-mode resonant DC-DC converter is widely used. Generally, the current-mode resonant DC-DC converter is controlled by PFM control which varies switching frequency. PFM control is valid for the control of the resonant converters in kHz level switching operation. However, in MHz level operation with PFM control, the output voltage of the resonant converter is hard to be controlled without large inductance.

For example, open loop characteristics of MHz level PFM control of LLC resonant DC-DC converter is shown in Fig. 1. From Fig. 1 (a), it can be seen that the switching frequency can't control the output voltage with relatively small inductance; 10nH of leakage inductance and 80nF of resonant capacitance. On the other hand, from the Fig. 1 (b), it can be seen that the switching frequency can control the output voltage with relatively large inductance; 10nH of leakage inductance, 100nH of additional inductance, and 4nF of resonant capacitance. Then, the size of the core of additional inductance is 14*5*5mm, which means interfere of the miniaturization of the circuit. From the reason, it seems that the MHz level operation with PFM control cannot be appropriate. Therefore, in this paper, the MHz level operation with PWM control for the current-mode resonant DC-DC converter is proposed.

III. Operational Principles of The Proposed Control Technique

A. Circuit Topology

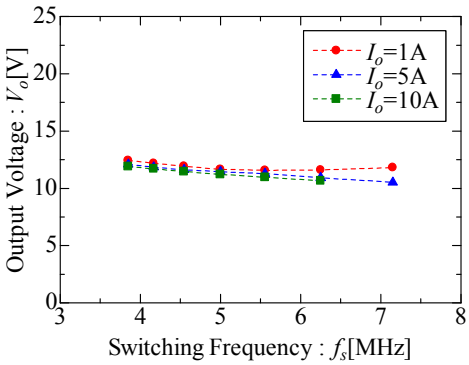
The circuit topology is based on a half-bridge type current-mode resonant converter as shown in Fig. 2. The primary-side is the half-bridge topology. Q_1 and Q_2 are driven in 50% duty ratio, alternatively. C_{oss1} and C_{oss2} are parasitic capacitance of primary-side switches Q_1 and Q_2. C_{r1} and C_{r2} are the resonant capacitors which have same capacitances and also make averaged voltage of v_c to a half of the input. The inside of the broken line is the magnetic transformer which equivalently indicated that L_r is leakage inductor, and L_m is the transformer's magnetizing inductance. The turn ratio is n : 1. L_r is used as the resonant inductor. The secondary-side is the full-bridge topology composed with diodes D_1 and D_2 for high-side arm switches, and transistors Q_3 and Q_4 for low-side arm switches.

B. Analysis of the Circuit Operation

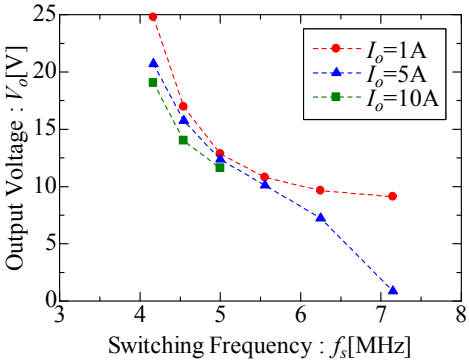
To simplify analysis of the circuit operation, the following assumptions are made:

- FETs are treated an ideal switch;
- The body diodes of the primary-side FET are neglected;
- The output capacitances of the primary-side FETs are constant during operation, satisfying $C_{oss1} = C_{oss2}$, $C_{oss} = C_{oss1} + C_{oss2}$;
- Resonant capacitances are satisfied $C_{r1} = C_{r2}$, $C_r = C_{r1} + C_{r2}$;
- The forward voltage drop and the parasitic capacitance of the secondary-side diodes are neglected;
- The output capacitance and the body diodes of the secondary-side FETs are neglected;
- The output voltage is constant;

The output voltage can be controlled with changing the duty ratio of Q_3 and Q_4, simultaneously. When the duty ratio is less than 0.5, the circuit is operated as well as conventional current resonance circuit. When the duty ratio is more than 0.5, the circuit is operated in the proposed operation.



(a) 10nH of leakage inductance and 80nF of resonant capacitance.



(b) 10nH of leakage inductance, 100nH of additional inductance and 4nF of resonant capacitance.

Figure 1. Open loop characteristics of LLC resonant DC-DC converter.

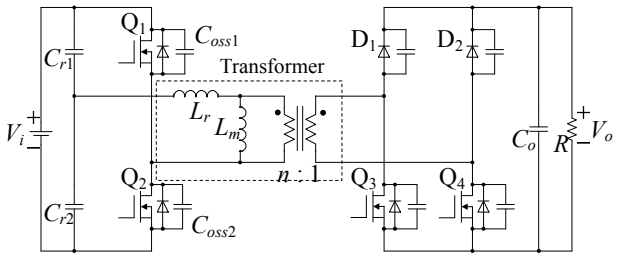


Figure 2. Circuit topology.

The circuit can be separated into 5 states in proposed operation with the switch combination. The definitions of the duty ratio D is followed as

$$D = T_{on}/T_S \ , \tag{1}$$

$$D = 1/2 + D_1 + D_4 + D_5 \ , \tag{2}$$

$$D_1 + D_2 + D_3 + D_4 + D_5 = 1/2 \tag{3}$$

and

$$\begin{cases} D \le 0.5 \cdots\cdots\cdots (\text{conventional operation}) \\ D > 0.5 \cdots\cdots\cdots (\text{proposed operation}) \end{cases} \tag{4}$$

where T_s is the switching period, and T_{on} is the on-term of Q_3 and Q_4. D_1~D_5 are the duty ratio of the each state.

The operation has two operation modes. One is discontinuous conduction mode (DCM). And, the other is continuous conduction mode (CCM). The condition of the two modes can be defined with

$$\begin{cases} D_2 < 1/2 - D_1 - D_4 - D_5, \ D_3 \ne 0 \cdots\cdots (\text{DCM}) \\ D_2 = 1/2 - D_1 - D_4 - D_5, \ D_3 = 0 \cdots\cdots (\text{CCM}) \end{cases} . \tag{5}$$

The operation waveforms with DCM are shown in Fig. 3. The definitions of the resonant are followed;

$$\omega_o = 1/\sqrt{L_r C_r} \ , \tag{6}$$

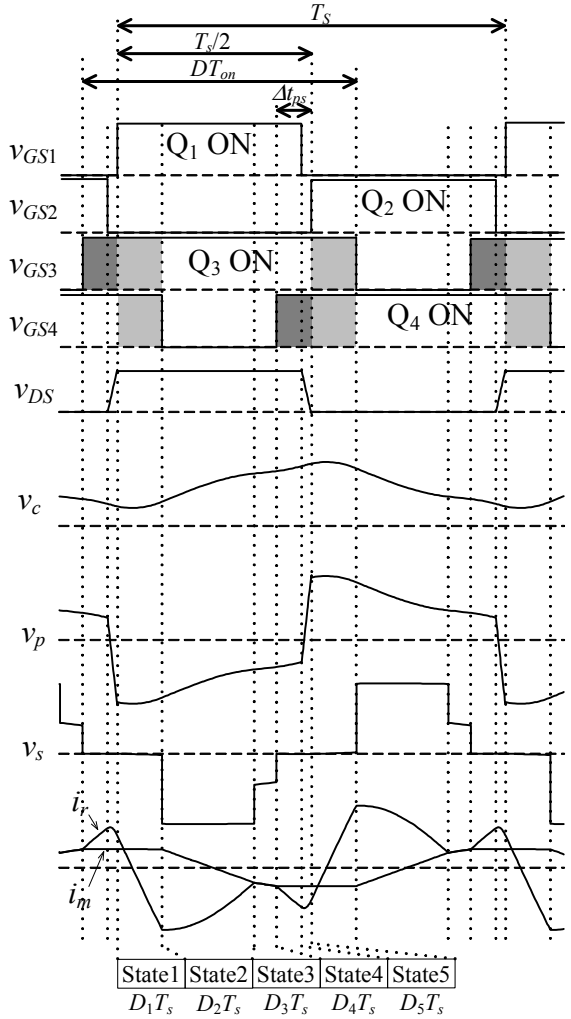
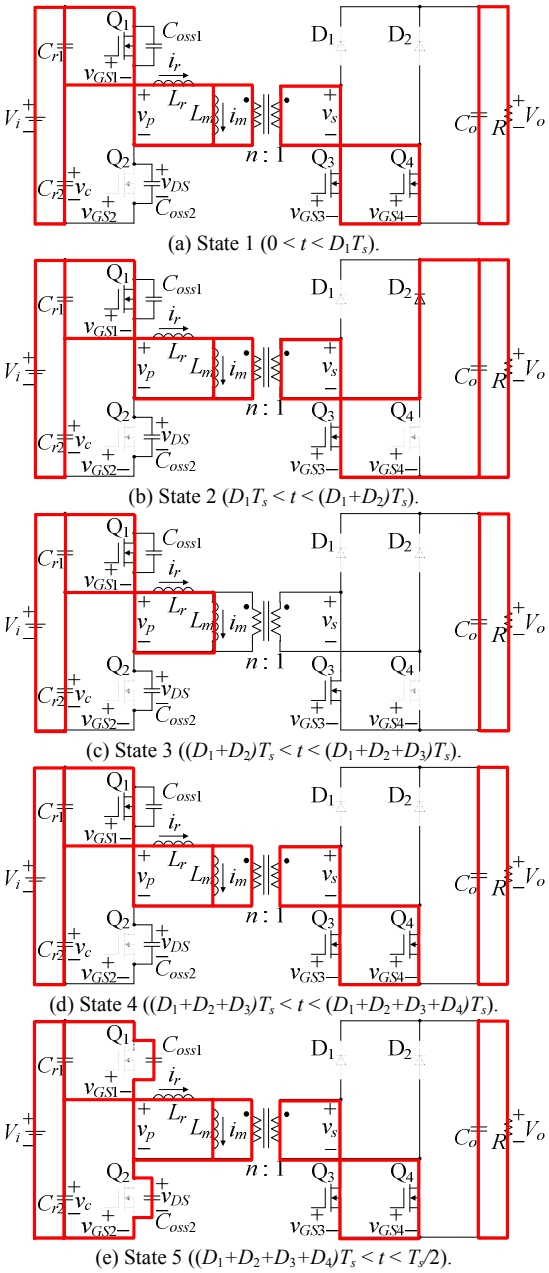


Figure 3. The operation waveforms.

TABLE I. CIRCUIT OPERATION STATES

State	FET				Diode	
	Q_1	Q_2	Q_3	Q_4	D_1	D_2
State 1	ON	OFF	ON	ON	OFF	OFF
State 2	ON	OFF	ON	OFF	OFF	ON
State 3	ON	OFF	ON	OFF	OFF	OFF
State 4	ON	OFF	ON	ON	OFF	OFF
State 5	OFF	OFF	ON	ON	OFF	OFF



(a) State 1 ($0 < t < D_1T_s$).

(b) State 2 ($D_1T_s < t < (D_1+D_2)T_s$).

(c) State 3 ($(D_1+D_2)T_s < t < (D_1+D_2+D_3)T_s$).

(d) State 4 ($(D_1+D_2+D_3)T_s < t < (D_1+D_2+D_3+D_4)T_s$).

(e) State 5 ($(D_1+D_2+D_3+D_4)T_s < t < T_s/2$).

Figure 4. The equivalent circuits for each state.

$$Z_r = \sqrt{L_r / C_r}\ , \tag{7}$$

$$\omega_1 = 1/\sqrt{(L_r + L_m)C_r}\ , \tag{8}$$

$$Z_1 = \sqrt{(L_r + L_m)/C_r} \tag{9}$$

and

$$\omega_{oss} = 1/\sqrt{L_r C_{oss}}\ . \tag{10}$$

The definitions of the initial value of the variable are followed;

$$v_{c1}(0) = V_i/2 - V_c \tag{11}$$

and

$$i_{r1}(0) = I_r\ . \tag{12}$$

The relations for the switch condition and the circuit operation states are summarized in TABLE I. The equivalent circuits for each state of a half switching term are shown in Fig. 4. In this figure, the switches drawn with weak colors represent OFF, and red line represents current flow. The description for each state is described below.

State 1($0 < t < D_1T_s$): In this state, t_1 is defined as $t_1=t$. The primary-side switch Q_1 is turned ON. Also, the secondary-side switches both Q_3 and Q_4 are turned ON. Q_3 and Q_4 are overlapped as indicated with the light gray area in Fig. 3. The leakage inductance L_r is magnetized by i_r for boosting output voltage. From the figure, $v_{c1}(t_1)$ and $i_{r1}(t_1)$ are became

$$v_{c1}(t_1) = V_i - \{(V_i/2 + V_c)\cos(\omega_o t_1) + Z_r I_r \sin(\omega_o t_1)\} \tag{13}$$

and

$$i_{r1}(t_1) = -1/Z_r\,(V_i/2 + V_c)\sin(\omega_o t_1) + I_r \cos(\omega_o t_1)\,. \tag{14}$$

The final values of the State 1 are

$$V_{c2} = v_{c1}(D_1T_S) \tag{15}$$

and

$$I_{r2} = i_{r1}(D_1T_S)\,. \tag{16}$$

State 2($D_1T_s < t < (D_1+D_2)T_s$): In this state, t_2 is defined as $t_2=t-D_1T_s$. After Q_4 is turned OFF, the direction of the voltage applied to D_2 is inverted, and diode of D_2 becomes ON. The inductance current which is magnetized in state 1 flow through diode D_2 and switch Q_3, to the load. From the figure, $v_{c2}(t_2)$ and $i_{r2}(t_2)$ are became

$$\begin{aligned} v_{c2}(t_2) &= V_i - nV_o \\ &+ (V_{c2} - V_i + nV_o)\cos(\omega_o t_2) - Z_r I_{r2} \sin(\omega_o t_2) \end{aligned} \tag{17}$$

and

$$\begin{aligned} i_{r2}(t_2) &= 1/Z_r\,(V_{c2} - V_i + nV_o)\sin(\omega_o t_2) \\ &+ I_{r2}\cos(\omega_o t_2) \end{aligned}\ . \tag{18}$$

The final values of the State 2 are

$$V_{c3} = v_{c2}(D_2T_S) \tag{19}$$

and

$$I_{r3} = i_{r2}(D_2T_S)\,. \tag{20}$$

State 3($(D_1+D_2)T_s < t < (D_1+D_2+D_3)T_s$): In this state, t_3 is defined as $t_3=t-D_1T_s-D_2T_s$. The direction of the diode D_2 current is inverted, and diode of D_2 becomes OFF. In the state, resonant current i_r equal to magnetizing current i_m. From the figure, $v_{c3}(t_3)$ and $i_{r3}(t_3)$ are became

$$v_{c3}(t_3) = V_i + (V_{c3} - V_i)\cos(\omega_1 t_3) - Z_1 I_{r3} \sin(\omega_1 t_3) \tag{21}$$

and

$$i_{r3}(t_3) = 1/Z_1\,(V_{c3} - V_i)\sin(\omega_1 t_3) + I_{r3}\cos(\omega_1 t_3)\,. \tag{22}$$

The final values of the State 3 are

$$V_{c4} = v_{c3}(D_3T_S) \tag{23}$$

and

$$I_{r4} = i_{r3}(D_3T_S)\,. \tag{24}$$

State 4($(D_1+D_2+D_3)T_s < t < (D_1+D_2+D_3+D_4)T_s$): In this state, t_4 is defined as $t_4=t-D_1T_s-D_2T_s-D_3T_s$. This state is similar to State 1. In the state, the leakage inductance L_r is magnetized by i_r for ZVS operation. Q_3 and Q_4 are overlapped as indicated with the dark gray area in Fig. 3. From the figure, $v_{c4}(t_4)$ and $i_{r4}(t_4)$ are became

$$v_{c4}(t_4) = V_i + (V_{c4} - V_i)\cos(\omega_o t_4) - Z_r I_{r4} \sin(\omega_o t_4) \tag{25}$$

and

$$i_{r4}(t_4) = 1/Z_r\,(V_{c4} - V_i)\sin(\omega_o t_4) + I_{r4}\cos(\omega_o t_4)\,. \tag{26}$$

The final values of the State 4 are

$$V_{c5} = v_{c4}(D_4T_S) \tag{27}$$

and

$$I_{r5} = i_{r4}(D_4T_S)\,. \tag{28}$$

State 5($(D_1+D_2+D_3+D_4)T_s < t < T_s/2$): In this state, t_5 is defined as $t_5=t-D_1T_s-D_2T_s-D_3T_s-D_4T_s$. The primary-side switch Q_1 is turned OFF. All primary-side switches are turned OFF, called dead-time. The parasitic capacitor C_{oss1} of Q_1 is discharged by a half of resonant inductance current i_r. Q_3 and Q_4 are overlapped as indicated with the dark gray area in Fig. 3. From the figure, $v_{c5}(t_5)$, $v_{DS5}(t_5)$ and $i_{r5}(t_5)$ are became

$$\begin{aligned} v_{c5}(t_5) &= V_{c5} - \frac{\omega_o{}^2 (V_{c5} - V_i)}{\omega_o{}^2 + \omega_{oss}{}^2} \\ &+ \frac{\omega_o{}^2 (V_{c5} - V_i)}{\omega_o{}^2 + \omega_{oss}{}^2} \cos\left(\sqrt{\omega_o{}^2 + \omega_{oss}{}^2} \cdot t_5\right) \\ &- \frac{I_{r5}}{C_r \sqrt{\omega_o{}^2 + \omega_{oss}{}^2}} \sin\left(\sqrt{\omega_o{}^2 + \omega_{oss}{}^2} \cdot t_5\right) \end{aligned}\ , \tag{29}$$

$$v_{DS5}(t_5)=\frac{\omega_{oss}{}^2(V_{c5}-V_i)}{\omega_o{}^2+\omega_{oss}{}^2}+V_i$$
$$-\frac{\omega_{oss}{}^2(V_{c5}-V_i)}{\omega_o{}^2+\omega_{oss}{}^2}\cos\left(\sqrt{\omega_o{}^2+\omega_{oss}{}^2}\cdot t_5\right) \quad (30)$$
$$+\frac{I_{r5}}{C_{oss}\sqrt{\omega_o{}^2+\omega_{oss}{}^2}}\sin\left(\sqrt{\omega_o{}^2+\omega_{oss}{}^2}\cdot t_5\right)$$

and

$$i_{r5}(t_5)=\frac{V_{c5}-V_i}{L_r\sqrt{\omega_o{}^2+\omega_{oss}{}^2}}\cdot\sin\left(\sqrt{\omega_o{}^2+\omega_{oss}{}^2}\cdot t_5\right) \quad (31)$$
$$+I_{r5}\cos\left(\sqrt{\omega_o{}^2+\omega_{oss}{}^2}\cdot t_5\right)$$

C. *The Method for Achieving ZVS*

The proposed operation does not achieve ZVS with controlling dead-time as well as the conventional operation. As shown in Fig. 3, the proposed operation has phase-shift between primary and secondary-side switches. Δt_{ps} is the time length of the phase-shift. Without the phase-shift, Δt_{ps}=0ns, the previous state of the dead-time becomes discontinuous current state. With this situation, initial current cannot be charged enough for ZVS because of secondary parasitic capacitance. Therefore, even with the long dead-time term, ZVS cannot be achieved. With phase-shift, the problem of the initial current can be solved. From eqs. (26) and (28), the initial current of the dead time, I_{r5}, is

$$I_{r5}=1/Z_r(V_{c4}-V_i)\sin(\omega_o D_4 T_S)+I_{r4}\cos(\omega_o D_4 T_S). \quad (32)$$

The term of the phase-shift becomes

$$\Delta t_{ps}=D_4T_S+D_5T_S. \quad (33)$$

In eq. (33), as defined as the D_5T_s is fixed, the term of state 4 becomes larger with the increase of Δt_{ps}. For an example, in the conditions of C_{oss}=900pF, V_i=36V, R=1.5ohm, D_5T_s=5ns, the relation of Δt_{ps} and I_{r5} are shown in Fig. 5. From this figure, it can be seen that I_{r5} is related to Δt_{ps} almost linearly. With the enough amount of I_{r5}, the amount of electrical charge q_{r5} which flows leakage inductance in dead-time becomes larger as shown in Fig. 6 (a). The electrical charge q_{r5} can be calculated with

$$q_{r5}=\int_0^{D_5T_S} i_{r5}(t)dt. \quad (34)$$

For achieving ZVS, q_{r5} has to be larger than the amount of the electrical charge of the parasitic capacitance of the switch as

$$|q_{r5}|>q_{oss}. \quad (35)$$

where $q_{oss}=C_{oss}V_i$.

Under the condition with mentioned in above, $v_{DS5}(D_5T_S)$ can be decreased with the enough Δt_{ps} as shown in Fig. 6 (b). Therefore, with the condition of

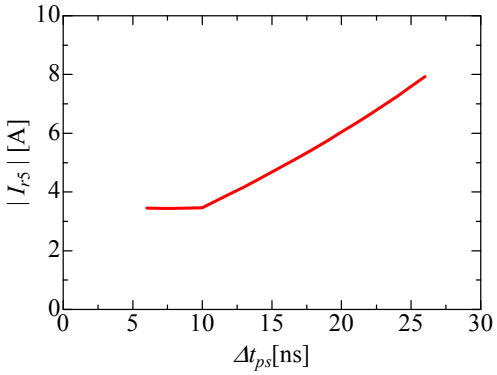
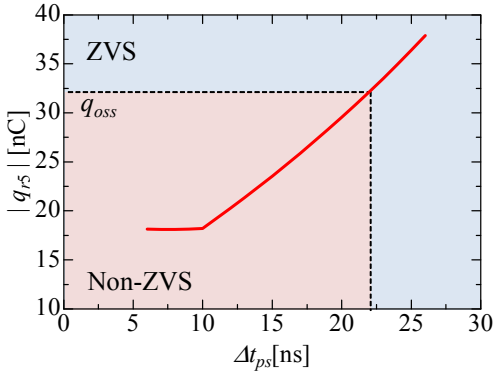
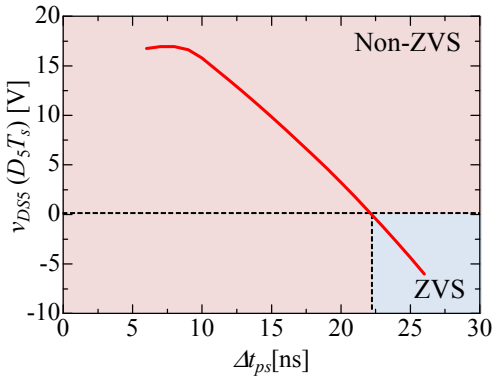


Figure 5. Δt_{ps} vs | I_{r5} |.



(a) Δt_{ps} vs | q_{r5} |.



(b) Δt_{ps} vs $v_{DS}(D_5T_S)$.

Figure 6. The effect of the phase-shift.

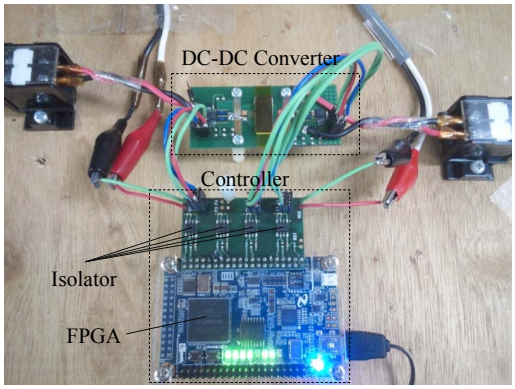


Figure 7. Prototype system for the experiments.

$$v_{DS5}(D_5T_S)<0\,, \tag{36}$$

the ZVS operation can be achieved.

From the mentioned above, it can be seen that the phase-shift Δt_{ps} between primary and secondary-side switches are valid for ZVS operation for the proposed PWM control.

IV. Experimental Results

The prototype system for the experiments is shown in Fig. 7. As a prototype digital controller, field programmable gate array (FPGA) Cyclone IV is used, which generates individual gate signal for each switches. The on-term of the gate signals are manually changed with software. The resolution of the gate signals is 1ns.

Some experiments have been carried out with parameters as shown in TABLE II, and 12V of constant output voltage with open loop control. Components used in the experiment are shown in TABLE III. As the primary side GaN-FETs, EPC2001 whose voltage rating is 100V, is used. As the secondary side GaN-FETs, EPC2015 whose voltage rating is 40V, is used. LM5113 is used as a gate driver for half-bridge-connected GaN-FETs.

The main circuit of the proposed 5MHz DC-DC converter is shown in Fig. 8. The total volume of the main circuit of the proposed 5MHz DC-DC converter is 16.14cm^3, where depth and width are 3.00cm and 6.81cm, and highest point is 0.79cm. The selection reason of the switches and magnetic transformer materials are described in [1].

The open loop static characteristics of the 5MHz PWM-controlled DC-DC converter are exhibited. From Fig. 9, it can be seen that voltage transfer ratio is controlled by duty ratio.

Figure 10 shows the waveforms of CCM mode and DCM mode with the phase-shift. The red dotted line shows achieving ZVS operation and red arrow shows enough initial current of the dead-time.

The maximum power efficiency is 89.4% from the Fig. 11. ZVS operation has been confirmed in the range of the experimental conditions. It is hard to measure the distribution of the power loss of this circuit because of the high power-density. Instead of power measurement, thermographic image as shown in Fig. 12, has been taken of the breadboard at point A in Fig. 11. From the results, the temperature of the secondary-side is still in high level. It is mentioned that the large secondary current and large duty ratio affects the loss of secondary side which is conduction loss of secondary-side diodes and FET. To improve the secondary-side large loss, synchronous rectifier will be applied in the future. The primary-side temperature is relatively low.

V. Conclusion

In this paper, a novel control technique and maintaining ZVS operation for the current-mode resonant converter in MHz level operation has been proposed. Some experiments have been done with the resonant converter regulated by PWM at 5MHz of switching frequency. Maximum power efficiency is 89.4%. ZVS operation has been confirmed with some experiments. The temperature of the secondary side is still in high level because of the large secondary current and large duty ratio. Though, the primary-side temperature is relatively low because of ZVS operation by phase-shift.

As the future work, analysis of boost-mode operation with phase-shift, realization of the wide control range, defining the

TABLE II. EXPERIMENTAL PARAMETERS

Specifications	Value
Input voltage: V_i	36V～44V
Output reference voltage: V_o	12V
Transformer ratio n : 1	2 : 1
Switching frequency: f_s	5MHz
Resonant frequency: f_r	4.98MHz
Transformer leakage inductance: L_r	33nH
Transformer magnetizing inductance: L_m	200nH
Resonant capacitor: C_{r1},C_{r2}	15.5nF
Output capacitor: C_o	18.8μF

TABLE III. EXPERIMENTAL COMPONENTS

Name	Manufacture	Part Name/ Material
Primary side GaN-FET	EPC	EPC2001
Secondary side GaN-FET	EPC	EPC2015
FET Driver	TEXAS INSTRUMENTS	LM5113
Diode	DIODES	PDS1040L
Transformer Core Material	TDK	NiZn Ferrite Core
Resonant Capacitor	TDK	C1608C0G1H392J
Input Capacitor	TDK	C3216X7R1H105K
Output Capacitor	TDK	C2012X7R1E475M
FPGA	Terasic (ALTERA)	DE0-nano (Cyclone IV)
Isolator	TEXAS INSTRUMENTS	ISO722

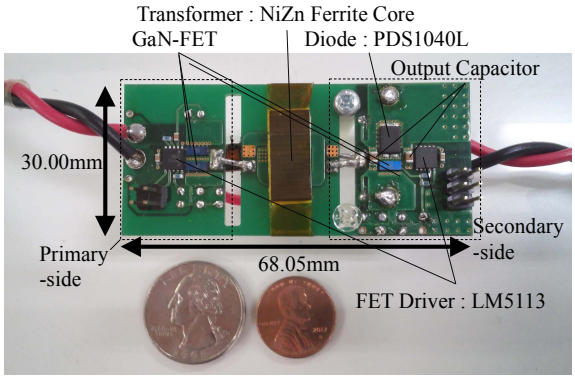


Figure 8. The main circuit of the converter.

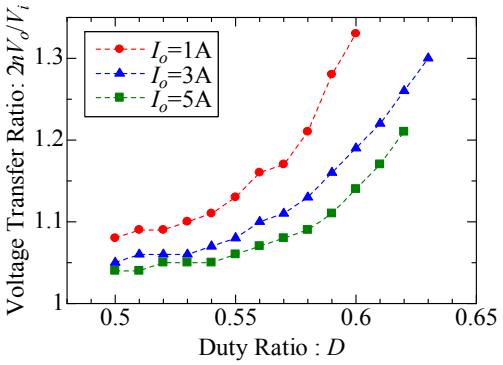


Figure 9. The open loop static characteristics of the converter.

optimal operation range of the converter, adapting secondary-side synchronous rectifier which leads higher power-efficiency, and feedback control by digital controller are under considerations.

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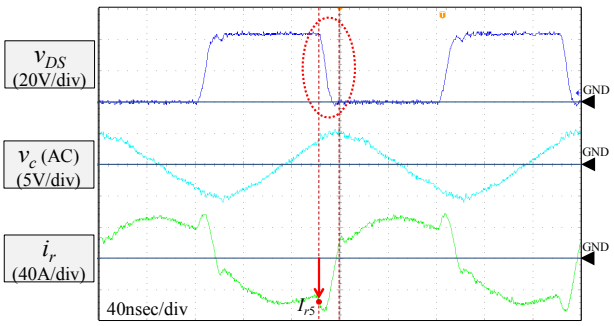
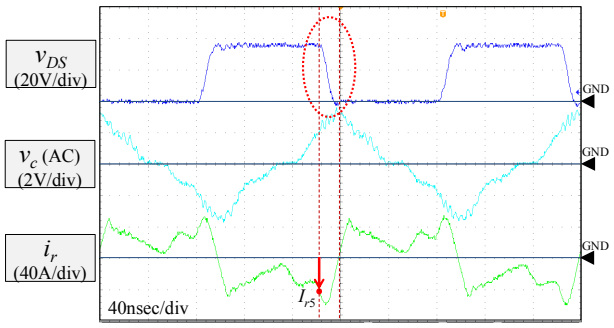


(a) CCM at V_i=44V, I_o=6.3A, D=0.6, Δt_{ps}=13ns.



(b) DCM at V_i=36V, I_o=2.8A, D=0.63, Δt_{ps}=14ns.

Figure 10. Experimental waveforms.

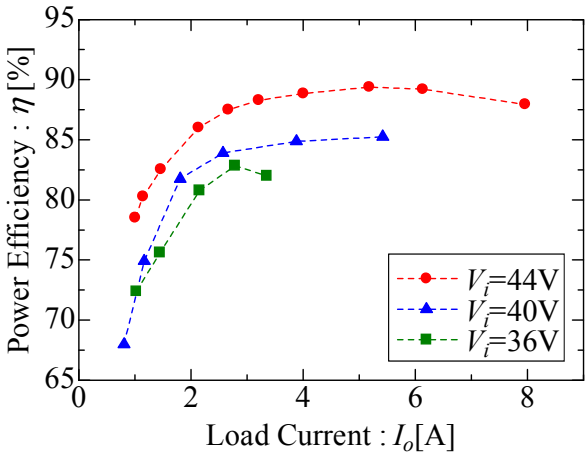


Figure 11. Power efficiency of the converter at V_o=12V.

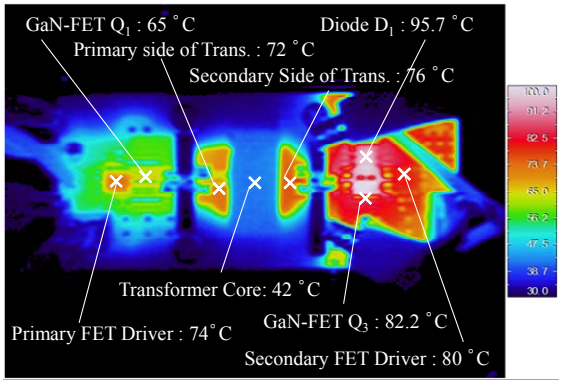


Figure 12. Thermographic image of the breadboard at point A in Fig. 11.