Surge Snubber Design for High Power-Density DC-DC Converters in HVDC Power Distribution Systems

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***Abstract*—In an isolated DC-DC converter utilized in the HVDC power distribution system, a large surge voltage occurs across the secondary-side diodes due to the transformer's leakage inductance, and then the diodes with a large withstand voltage are required. However, those diodes cause a lot of power loss. In this paper, a simple surge snubber with prominent surge suppression capability is examined, and the surge-voltage evaluation through the analysis using the high-frequency equivalent circuits, which is followed by the experimental confirmation. Furthermore, the the optimum design of its surge-snubber capacitor is presented.**

Keywords-component; HVDC power distribution system; isolated DC-DC converter; surge analysis; high-freaquency equivalent circuit; surge-snubber capacitor

I. INTRODUCTION

Recently the rapid growth of internet traffic has increased the number of ICT equipment in data centers. This results in the increase of electric power consumption in tele-communication buildings including data centers. The conventional data center utilizes the power distribution system based on the combined power lines of AC and 48VDC. On the other hand, the power distribution system using High-Voltage Direct-Current (HDVC) e.g. 400V, has several advantages such as higher efficiency due to reducing the number of conversion stages, and easier installation due to finer power cables. Recently this HVDC power distribution system has been researched and prepared for the practical application[1]. However, some difficulties have to be solved concerning a semiconductor circuit breaker and a high power-density isolated DC-DC converter. This paper discusses the surge-voltage occurrence related to diode's recovery characteristics in a high power-density isolated DC-DC converter. This surge voltage deteriorates or breaks down the diodes with lower withstand voltage. On the other hand, when the diodes with extremely high withstand voltage are utilized, a large amount of power loss is dissipated due to the high on-voltage. In order to realize a high power-density converter with highest efficiency and smallest size, the optimum selection of surge snubber and diodes through the surge-voltage evaluation is necessary.

Firstly in this paper, the surge voltage across the secondary-side diode is analyzed by deriving high-frequency equivalent circuits including some parasitic parameters such as the transformer's leakage inductance, the diode's depletion capacitance, the diode's equivalent stored electric charge, etc. As a result, the exact equations evaluating the surge voltage have been analytically derived, and have been experimentally confirmed.

Secondly, a simple surge snubber using a capacitor, which was proposed in the previous paper[2], is examined, and its prominent effect on the surge suppression is analyzed. Then, the optimum snubber design is discussed.

II. HIGH POWER-DENSITY ISOLATED DC-DC CONVERTER

A block diagram of the HVDC power distribution system is shown in Fig.1. The first stage consists of a power-factor-correction (PFC) converter for the harmonic reduction of input current waveform. The subsequent DC-DC converter operates for the dc-isolation and the voltage regulation. A typical circuit topology of the high power converter is a full-bridge type shown in Fig.2, where the output-voltage regulation is performed by the phase-shift driving of two pairs of switches.

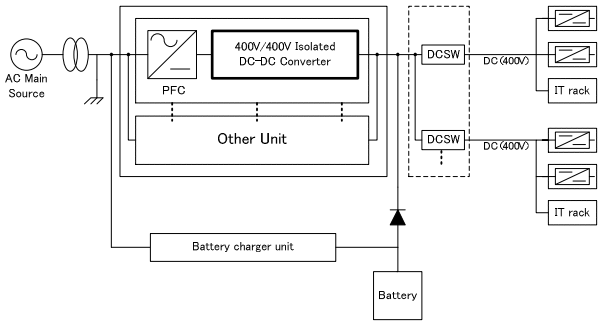

Fig.1. Block diagram of HVDC power distribution system with PFC converter and 400V/400V isolated DC-DC converter.

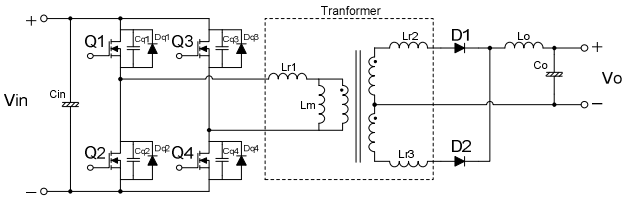

Fig.2. Circuit topology of full-bridge isolated DC-DC converter

III. SURGE ANALYSIS BY HIGH-FREQUENCY EQUIVALEVT CIRCUIT

In the full-bridge isolated DC-DC converter shown in Fig.2, big surge voltages occur across the secondary-side diodes during their turn-off times as shown in Fig.3. The causes of the surge occurrence are the transformer's leakage inductance and the diode's reverse current. Then a high-frequency equivalent circuit for the surge occurrence is shown in Fig.4. From this equivalent circuit, the peak value of the diode surge voltage is evaluated as follows[3,4]:

$$v_{d2\_peak} = 2\frac{Vin}{n} + 2\cdot\sqrt{\frac{Vin^2}{n^2} + \frac{Qd\cdot Vin}{n\cdot Cd}} \qquad (1)$$

where V_{in}: input voltage,
n: winding turns ratio of transformer,
Qd : equivalent stored electric charge in the diode,
Cd: depletion capacitance of diode.

It is clarified from (1) that the diode's surge voltage depends heavily on the input voltage and that its peak value may be higher than five times of the input voltage. For example, when the input voltage is 400V, the surge voltage may be over 2000V and then the diode breaks down. In order to protect the converter operating at higher voltage, some surge suppression techniques are necessary for the practical application.

IV. SURGE SNUBBER

The simple surge snubber using a single capacitor only has been proposed in the previous paper[2]. The full-bridge isolated DC-DC converter equipped with this snubber capacitor is shown in Fig.5. By applying the snubber capacitor Cs of 1μF, the diode's surge voltage is completely suppressed as shown by the experimental waveforms in Fig.6. In case without the snubber capacitor, the diode's reverse recovery is operated by the reverse voltage twice as higher as the input voltage, and a big surge voltage occurs as shown above. On the other hand, in case with the snubber capacitor, the diode's reverse recovery occurs under the lower voltage across the capacitor Cs during the dead-time period of primary switches. Furthermore, the generated higher-frequency(>10MHz) surge voltage is attenuated during the dead-time period. As a result, its peak value becomes lower than the steady-state value. However, when applying a snubber capacitor of smaller capacitance, another lower-frequency(2MHz) surge voltage appears due to another resonance as shown in Fig.7, though the higher-frequency surge mentioned above is suppressed during the dead-time period. The surge occurrence in the converter with a snubber capacitor is analyzed in the next section.

V. SURGE EVALUATION FOR THE CONVERTER WITH SNUBBER CAPACITOR

As the initial condition of surge occurrence, consider the circuit state during the dead time. All the primary switches and secondary diodes are at off-state as shown in Fig.8. During this dead time, the diode's reverse recovery occurs and the surge arises, but this surge voltage is sufficiently suppressed during the dead-time period as mentioned above. Then move on the next state shown in Fig.9, where primary switches Q1 and Q4

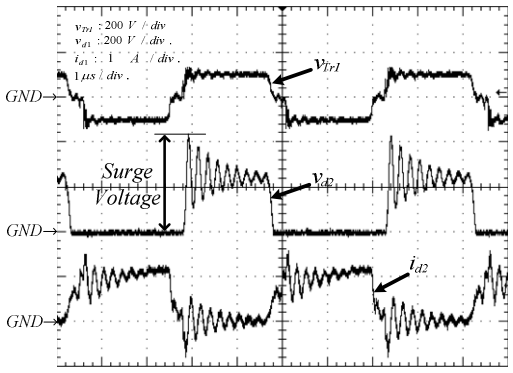

Fig.3. Experimental waveform of surge occurrence.

v_{Tr1} : transformer voltage
v_{d1} : secondary-side diode voltage
i_{d2} : secondary-side diode current
switching frequency : 200kHz

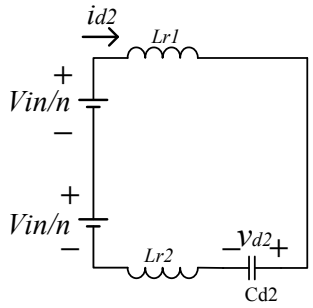

Fig.4. Equivalent circuit for analyzing

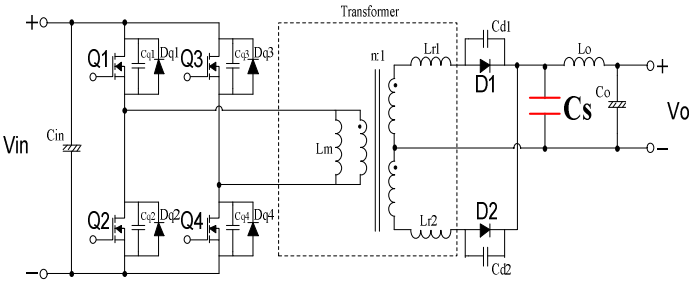

Fig.5. Full-bridge isolated DC-DC converter with Snubber Capacitor Cs

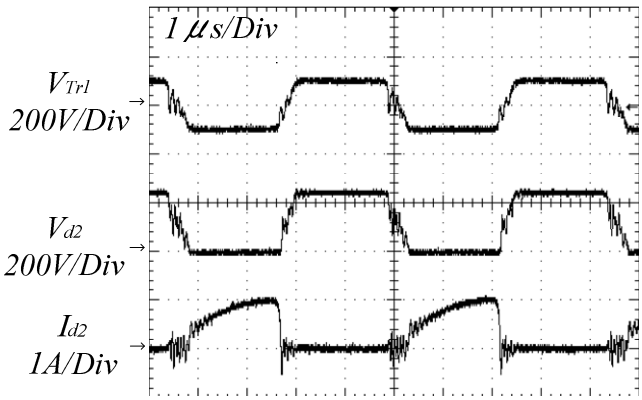

Fig.6. Experimental waveforms of surge occurrence (with snubber capacitance Cs=1.1μF).

are turned on. In this case, the surge current flows through leakage inductance Lr1 and snubber capacitor Cs, and the surge voltage appears across the diode D2 as a transient response. This surge voltage is analyzed by using the equivalent circuit shown in Fig.10. The circuit equations are derived as follows:

$$V_i = Lr \cdot \frac{di_{Lr1}}{dt} + v_{CS} \tag{2}$$

$$Cs \cdot \frac{dv_{CS}}{dt} = i_{Lr1} - I_O \tag{3}$$

$$V_i + v_{CS} = L_{r2} \cdot \frac{di_{Lr2}}{dt} + v_{d2} \tag{4}$$

$$i_{L2} = Cd \cdot \frac{dv_{d2}}{dt} \tag{5}$$

The initial conditions are defined as follows:

$$i_{Lr1}(0) = I_{Lr10}, i_{Lr2}(0) = I_{Lr20}, v_{CS}(0) = V_{CS0}, v_{d2}(0) = V_{d20}$$

Deriving the expression of diode's surge voltage v_{d2} from (2) ~ (5), it contains two frequency components: One is a higher-frequency component (>10MHz) associated with leakage inductance Lr2 and depletion capacitance Cd2, and the other is a lower-frequency component (2MHz) associated with leakage inductance Lr1 and snubber capacitor Cs. According to the experimental waveforms, the higher-frequency component is much smaller than the lower-frequency one. Then the peak value of the surge voltage is evaluated by the lower-frequency component, and is expressed as follows:

$$v_{d2\_peak} = \sqrt{\left[V_{CS} - \frac{V_{in}}{n}\right]^2 + \left\{\sqrt{\frac{L_{r2}}{Cs}} \cdot (I_{Lr10} - I_o)\right\}^2} + 2 \cdot \frac{V_{in}}{n} \tag{6}$$

where
- n: winding turns ratio,
- $Lr = Lr1 = Lr2$,
- Io: load current,
- Vcs: voltage across snubber capacitance,
- I_{L10} : current through leakage inductance.

Here, examine the relationship between voltage and capacitance value of snubber capacitor during the dead-time period. The equivalent circuit during the dead time is shown in Fig.11, where the load current is not supplied from the input power source, but is provided from the snubber capacitor Cs. As a result, the final value Vcs during the dead time is expressed as

$$V_{CS} = \frac{V_{in}}{n} - \frac{I_O}{Cs} \cdot T_D \tag{7}$$

where T_D: dead time

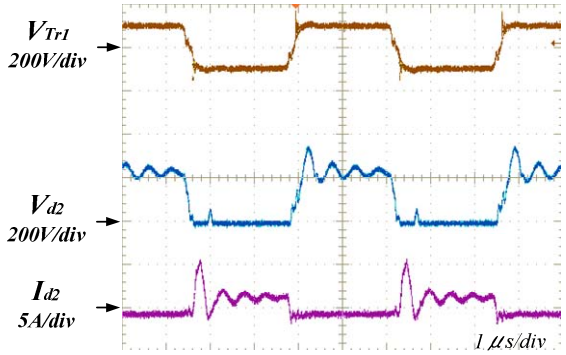

Fig.7. Experimental waveforms of surge occurrence (with snubber capacitance Cs=5nF)

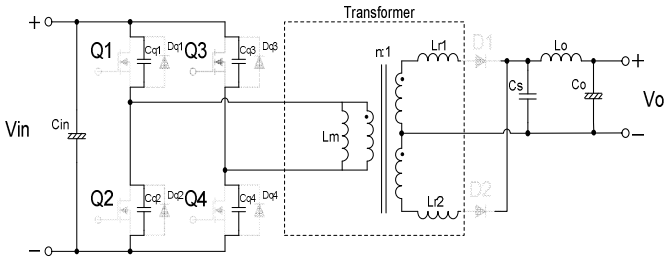

Fig.8. Circuit state during the dead time

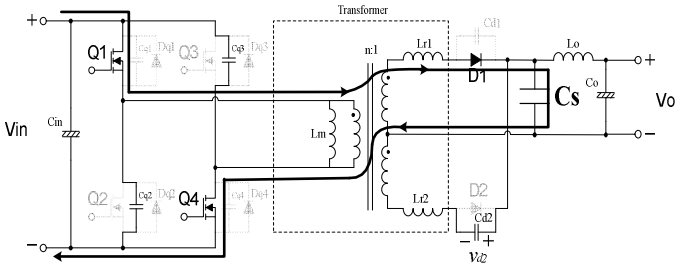

Fig.9. Surge current paths at turn-on time of primary switches

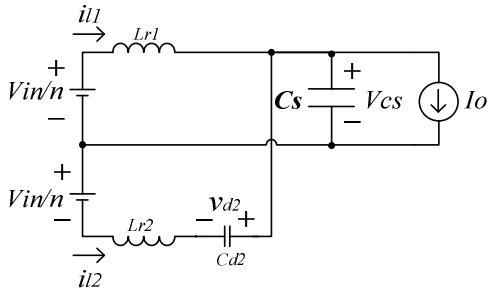

Fig.10. Equivalent circuit for surge current path at turn-on time of primary switches

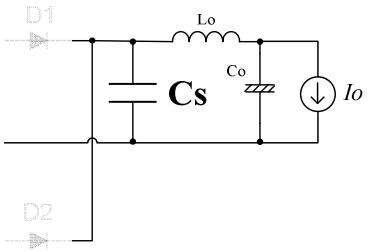

Fig.11. Equivalent circuit during the dead time

From (6) and (7), the peak value of the surge voltage is finally expressed as follows:

$$v_{d2\_peak} = \sqrt{\left[\frac{I_o}{Cs}\cdot T_D\right]^2 + \left\{\sqrt{\frac{Lr}{Cs}}\cdot\left(I_{Lr10} - I_o\right)\right\}^2} + 2\cdot\frac{V_{in}}{n} \qquad (8)$$

These analytical expressions (1) and (8) for the diode's surge voltage were confirmed by experiment as shown in Fig.12, where the snubber suppresses the surge voltage by half when compared with the original case without snubber.

VI. DESIGN OF SURGE-SNUBBER CAPACITOR

Here, examine the relationship between snubber capacitance and surge voltage. The experimental confirmation for the analytical expression (8) is shown in Fig.13, where the input voltage of 100V was used due to the experimental condition. As a result, an excellent coincidence has been obtained. Therefore, by using the equation (8), the minimum capacitance value for satisfactory surge suppression is determined for any cases of main circuit parameters and parasitic parameters such as transformer's leakage inductance and diode's depletion capacitance.

For example, if the surge suppression below 900V is required in case of input voltage 380V and load current 2A, it is clarified from Fig.13 that the snubber capacitance of more than 20nF is necessary.

VII. EFFECT OF SNUBBER CAPACITOR ON CONTROL CHARACTERISTICS

In the above discussions, a prominent effect of the snubber capacitor on surge suppression was mentioned, and the analytical expression for the snubber capacitor design has been derived. On the other hand, its effects on the other characteristics of the converter have to be examined.

Here, the effect of snubber capacitor on the control characteristics of the main converter is discussed. Typically the regulation of the full-bridge DC-DC converter is performed by "phase-shift control" as shown in Fig.14. The control parameter is the phase difference ϕ between turnoff times of switches Q1 and Q4. Changing this phase difference ϕ, the control characteristics without snubber capacitor is obtained as shown in Fig. 15. On the other hand, for the converter with snubber capacitor, the analytical expression of the output voltage is derived as follows:

$$V_O = \frac{V_i}{1 + \dfrac{4\cdot Lr\cdot I_O}{D^2\cdot T_S\cdot V_i}} - r_L\cdot I_O \qquad (9)$$

where

$$D = 1 - \frac{\phi}{180}$$

The control characteristics of the converter equipped with snubber capacitor is calculated as shown in Fig.16. As a result, the control characteristics are deteriorated under light load current.

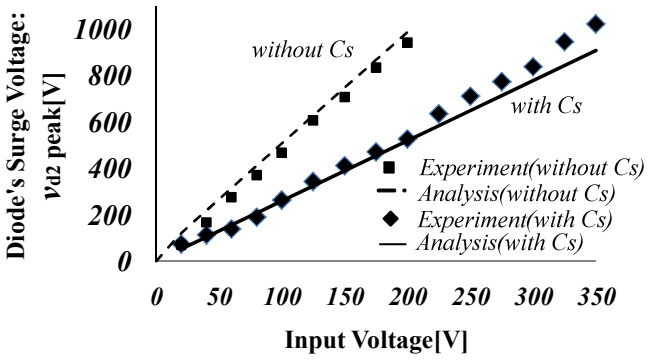

Fig.12. Analytical and experimental results for diode's surge voltage (Cs=50nF, Io=2A,Cd1=Cd2=200pF,Lr1=Lr2=Lr=2μH)

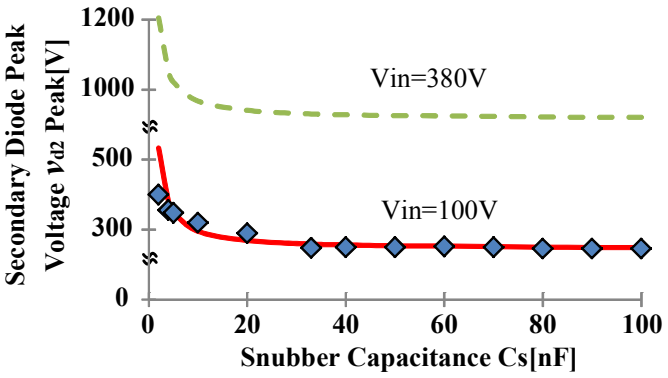

Fig.13. Effect of snubber capacitance on diode's surge voltage. (Comparison of analysis and experiment: Vin=100V, Io=2A, Cd1=Cd2=200pF, Lr=2μH)

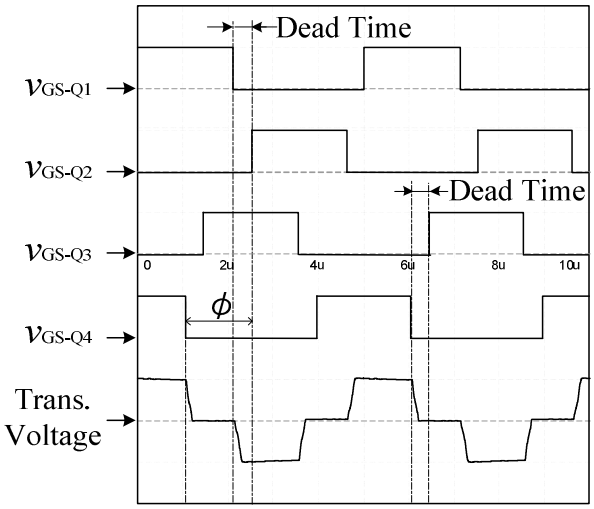

Fig.14. Gate-voltage pattern of primary switches Q1-Q4 for phase-shift control.

VIII. CONCLUSIONS

In this paper, a simple surge snubber with a prominent effect on the surge suppression was confirmed by the experiment and analysis. Also the design guideline of surge snubber has been derived by analyzing the equivalent circuit model. On the other hand, this snubber induces some defects to the control characteristics of the DC-DC converter, and the solution is future work.

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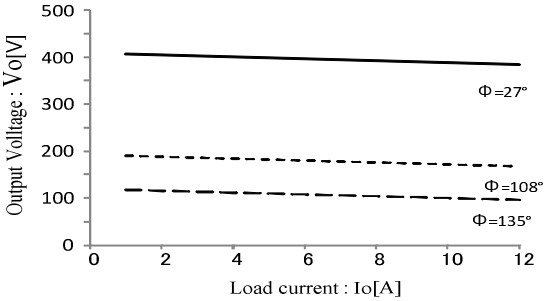

Fig. 15. Control characteristics of the converter without snubber capacitor Cs.

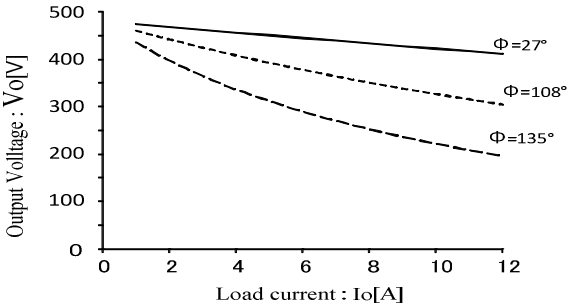

Fig.16. Control characteristics of the converter with snubber capacitor Cs.