

An Analysis of Bidirectional Superposed Dual Active Bridge DC-DC Converter with Synchronous Rectifier

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Abstract— This paper describes the principles and characteristics of a novel bidirectional superposed dual active bridge DC-DC converter with synchronous rectifier, which has a mechanism formed from two bridge-type converters that are linked through superposition in additive polarity in series. Conventionally, for an isolated dual active bridge DC-DC converter, the rated voltage of its switching elements is decided according to the DC power source voltage and load current. Therefore, as the voltage and current specifications of a DC-DC converter become higher, physical size becomes larger, conduction and switching losses increase and power efficiency reduces. To solve this problem, the authors devised the proposed DC-DC converter capable of lowering the rated voltage of switching elements, by means of sharing DC power source voltage and load current between two converters. Further, the capacity of the high frequency transformer becomes small, making the DC-DC converter more efficient and smaller. We designed and constructed a 1kW DC-DC converter prototype, and conducted performance evaluation testing. As a result, a conversion efficiency of 98.2% at a rated output of 1kW was obtained. A detailed analysis of power flow was also carried out, to identify the characteristics of the converter developed.

Keywords: bidirectional DC-DC converter; superposed dual active bridge, synchronous rectifier, ZCS-ZVS

I. INTRODUCTION

For isolated dual active bridge DC-DC converters which have been previously researched, various techniques to improve converter conversion efficiency have been applied: for instance, application of resonant type converter using snubber capacitance [1], uses of silicon carbide (SiC) power devices and new magnetic materials [2]. And isolated dual active bridge DC-DC converters have been applied for use in hybrid electric vehicles [3] and energy storage systems [4]. Power generation systems incorporating natural energy are generally equipped with secondary batteries and electric double-layer capacitors; and to control their charge/discharge operation, bidirectional DC-DC converters have also been widely employed [5].

In the pursuit of high energy efficiency for such equipment, bus voltage tends to be high along with development of high-tech switching devices, while in practical terms energy storage devices such as Li-ion batteries and electric double-layer capacitors cannot meet the high voltage requirements. Therefore, in the case that high voltage, high current

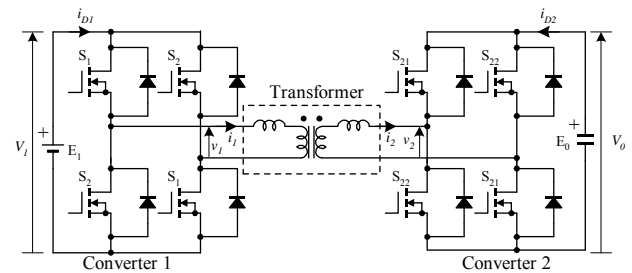


Fig. 1. Bidirectional isolated dual active bridge DC-DC converter.

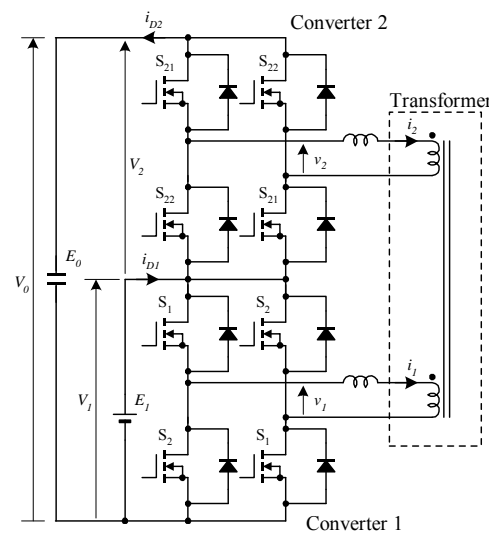


Fig. 2. Novel superposed dual active bridge DC-DC converter with synchronous rectifier.

specifications are required, DC-DC converters need to be large in size, resulting in a reduction in power efficiency due to an increase in conduction and switching losses. As a solution to this problem, the authors proposed a bidirectional superposed dual active bridge DC-DC converter equipped with a synchronous rectification function. The proposed converter, which has a mechanism formed from two bridge-type converters that are linked through superposition in additive polarity in series, is capable of lowering the rated voltage of switching elements, by means of sharing DC power source voltage and load current on the high-voltage side between the two converters [6]. Fig. 1 shows the circuit diagram of a conventional converter, and Fig. 2 shows the circuit diagram of

our proposed DC-DC converter. In Fig. 1, converter 1 is set on the low-voltage side, while converter 2 is set on the high-voltage side. The low-voltage side and high-voltage side are generally isolated; however, the conventional DC-DC converter has problems in that 1) the rated current of converter 1 switching elements are controlled by the DC current (i_{DI}), causing a high current condition; and 2) the rated voltage of converter 2 switching elements are controlled by the voltage (V_0) on the high-voltage side, causing a high voltage condition.

In contrast, the proposed converter has no function to isolate the input and output power circuits; however, it has the following beneficial characteristics:

- 1) The output voltage (V_0) of power source (E_0) on the high-voltage side can be shared by converters 1 and 2 based on the transformer winding turns ratio. For instance, when the turns ratio is 1:1, the rated voltage of switching elements of converters 1 and 2 is half of V_0 , contributing to the lowering of the switching element voltage rating.
- 2) The DC current (i_{DI}) passing through power source (E_I) on the low-voltage side can be shared by converters 1 and 2 based on the transformer winding turns ratio. For instance, when the turns ratio is 1:1, the rated current of switching elements of converters 1 and 2 is half of i_{DI} , contributing to the lowering of the switching element current rating.
- 3) Through mechanisms 1) and 2), the rated capacity to be processed by the transformer is decreased by half, contributing to downsizing as well as loss reduction.
- 4) Zero-current switching (ZCS) and zero-voltage switching (ZVS) are realized under a wide operation range when all switching elements are turned on, resulting in high efficiency.

II. OPERATING MODES OF THE PROPOSED DC-DC CONVERTER

Power flow from DC power source on the low-voltage side (E_I) toward DC power source on the high-voltage side (E_0) is defined as power running mode, while the opposite power flow is defined as power regenerative mode. Figs. 3 and 4 show transformer current waveforms at the time of DC-DC converter switching operation in power running and regenerative modes, respectively. An individual converter is driven in one-pulse mode without controlling pulse width. The on-duty ratio between S_1 and S_2 , as well as that between S_2 and S_{22} , is 50%.

Depending on the magnitude of current transmitted, and voltage magnitudes of DC power voltages (V_1 , V_2), transformer currents (i_1 , i_2) of DC-DC converter have three waveform patterns of current waveforms; that is, patterns (a), (b) and (c), as shown in Figs. 3 and 4. In the case of pattern (c) in both power running and regenerative modes, turn-on of all switching elements occurs under the condition of ZCS and ZVS, because the anti-parallel diode is in on-state. In contrast, the hard-turn-on phenomenon occurs in particular switching elements; that is, S_{21} and S_{22} in pattern (a), S_1 and S_2 in pattern (b) in power running mode, as well as S_1 and S_2 in pattern (a),

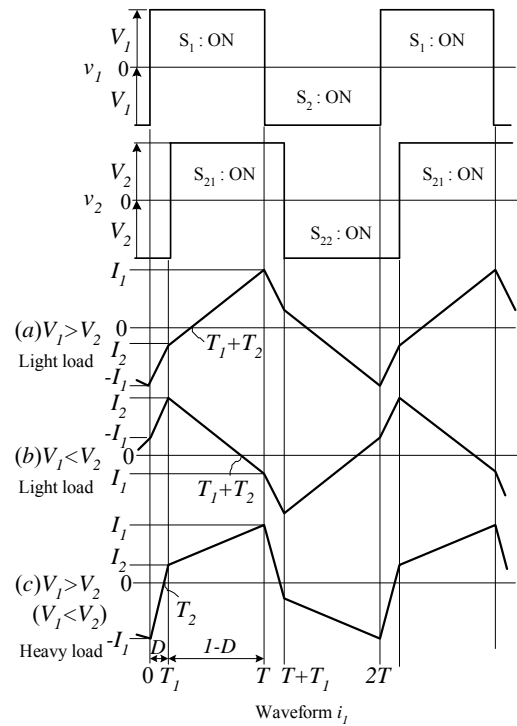


Fig. 3. Operating waveforms in power running mode.

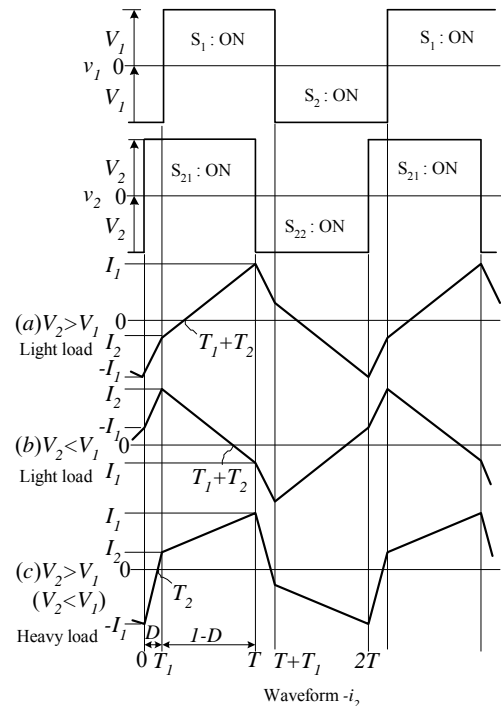


Fig. 4. Operating waveforms in power regenerative mode.

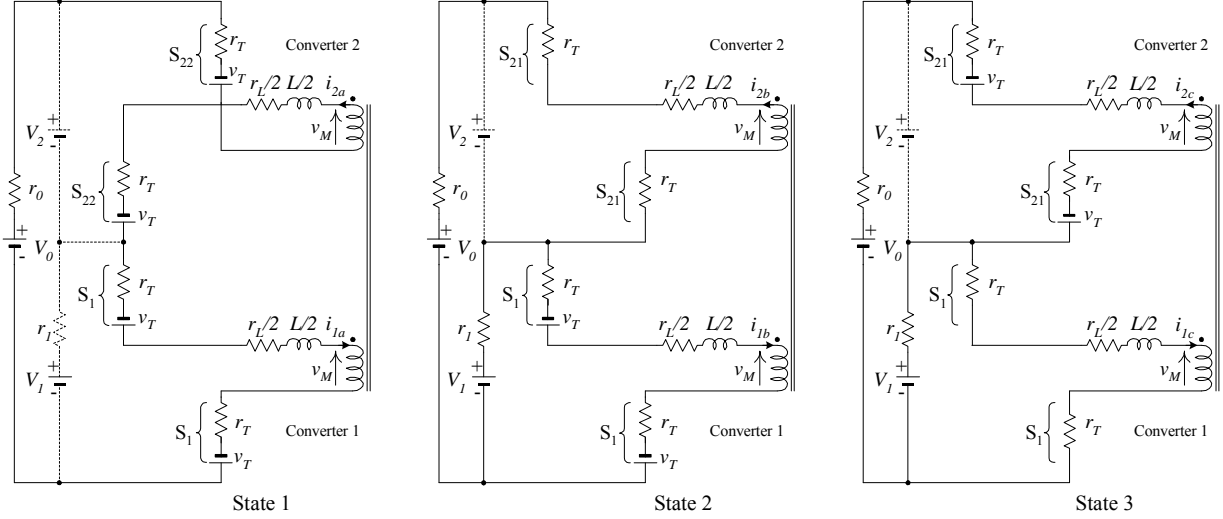


Fig. 5. Current flows and equivalent circuits.

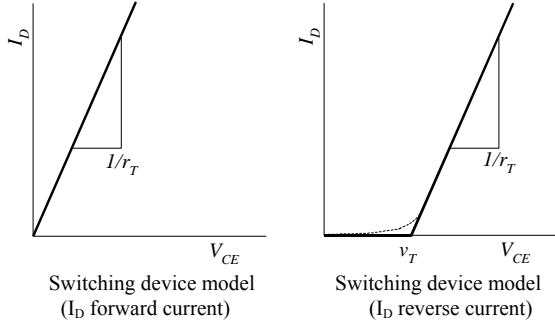


Fig. 6. MOSFET device models.

S_{21} and S_{22} in pattern (b) in power regenerative mode. In this case, however, the current flowing to switching elements is small, resulting in only a minor switching loss.

III. OPERATING ANALYSIS

In the case of pattern (a) in power running mode, states that emerged in the time periods $0 \sim T_1$, $T_1 \sim T_1 + T_2$, $T_1 + T_2 \sim T$ are defined as states 1, 2 and 3, respectively. To analyze power flow, we set up circuits equivalent to these states as shown in Fig. 5, and obtained MOSFET device models by applying the method of approximation, as shown in Fig. 6. Using the converter circuit parameters listed in Table 1, transformer primary current (i_1) was obtained from numerical calculations.

A. State Analysis

1) State 1 ($t = 0 \sim T_1$)

S_1 is turned on under the condition of $i_{1a} = i_{2a} = -I_1$ when $t = 0$, and then state 1 starts. At this time, diodes in an anti-parallel connection with S_1 are already in a turn-on condition. Since directions of current flows (i_{1a} , i_{2a}) do not change rapidly, i_{1a} flows to FET of S_1 , and i_{2a} flows to FET of S_{22} . Current does

not flow to DC power source (E_1). The following two Laplace transform equations are given by the equivalent circuit of state 1 shown in Fig. 5. Default values of i_{1a} and i_{2a} are set as $-I_1$.

$$\frac{V_0}{s} = \left(\frac{Ls + r_L}{2} + 2r_T + r_0 \right) I_{2a}(s) - \frac{2v_T}{s} + \frac{LI_1}{2} - V_M(s) + \frac{V_1}{s} \quad (1)$$

$$\frac{V_1}{s} = \left(\frac{Ls + r_L}{2} + 2r_T \right) I_{1a}(s) - \frac{2v_T}{s} + \frac{LI_1}{2} + V_M(s) \quad (2)$$

Since $i_{1a} = i_{2a}$, (3) is obtained from both (1) and (2).

$$I_{1a}(s) = I_{2a}(s) = \frac{V_0 + 4v_T - LI_1 s}{Ls \left(s + \frac{r_L + r_0 + 4r_T}{L} \right)} = \frac{\frac{V_{1a}}{r_a} - \frac{V_{1a} + I_1}{r_a}}{s + \frac{r_a}{L}} \quad (3)$$

Here, (4) is obtained from the following equations.

$$r_a = r_L + r_0 + 4r_T, \quad V_{1a} = V_0 + 4v_T$$

$$i_{1a}(t) = i_{2a}(t) = \frac{V_{1a}}{r_a} - \left(\frac{V_{1a}}{r_a} + I_1 \right) e^{-\frac{r_a}{L}t} \quad (4)$$

Further, when the current is defined as I_2 at time T_1 , and $T_1/T = D$, (5) is obtained from (4).

$$e^{-\frac{\pi r_a D}{\omega L}} = \frac{V_{1a} - I_2}{\frac{r_a}{V_{1a} + I_1}} \quad (5)$$

2) State 2 ($t = T_1 \sim T_1 + T_2$)

S_{21} is turned on when $t = T_1$ after S_{22} is turned off, and reverse recovery current flows until reverse recovery for diodes of S_{22} is completed, which causes DC voltage (V_2) to short-circuit. In this case, the hard-turn-on phenomenon of S_{21} occurs. However, this phenomenon emerges in the light load period, resulting in only a minor switching loss. In the case of pattern (c) in power running mode, when S_{21} is turned on under the condition that diodes of S_{21} are in on-state, resulting in the condition of ZCS and ZVS. In this mode, current of $i_{1b} + i_{2b}$ flows to DC power source (E_1). The following two Laplace transform equations are given by the equivalent circuit of state 2 shown in Fig. 5. Default values of i_{1a} and i_{2a} are set as I_2 .

$$\frac{V_0}{s} = -r_1 \{I_{1b}(s) + I_{2b}(s)\} - \left(\frac{Ls + r_L}{2} + 2r_T + r_0 \right) I_{2b}(s) + \frac{LI_2}{2} + V_M(s) + \frac{V_1}{s} \quad (6)$$

$$\frac{V_1}{s} = r_1 \{I_{1b}(s) + I_{2b}(s)\} + \left(\frac{Ls + r_L}{2} + 2r_T \right) I_{1b}(s) - \frac{2v_T}{s} - \frac{LI_2}{2} + V_M(s) \quad (7)$$

Since $i_{1b} = i_{2b}$, (8) is obtained from (6) and (7).

$$I_{1b}(s) = I_{2b}(s) = \frac{2V_1 - V_0 + 2v_T + LI_2 s}{Ls \left(s + \frac{r_L + 4r_T + r_0 + 4r_1}{L} \right)} = \frac{V_{1b}}{r_b} - \frac{V_{1b} - I_2}{s + \frac{r_b}{L}} \quad (8)$$

Here, (9) is obtained from the following equations.

$$r_b = r_L + 4r_T + r_0 + 4r_1, \quad V_{1b} = 2V_1 - V_0 + 2v_T$$

$$i_{1b}(t) = i_{2b}(t) = \frac{V_{1b}}{r_b} - \left(\frac{V_{1b}}{r_b} - I_2 \right) e^{-\frac{r_b t}{L}} \quad (9)$$

Further, when the current is defined as zero at time $T_1 + T_2$, (10) is obtained from (9).

$$e^{-\frac{\pi r_b T_2}{\omega L T}} = 1 - \frac{r_b}{V_{1b}} I_2 \quad (10)$$

3) State 3 ($t = T_1 + T_2 \sim T$)

The magnetic energy of leakage inductance diminishes when $t = T_1 + T_2$. The reverse current flowing to FET of S_1 is

turned to flow forward though FET of S_1 under the condition of ZCS and ZVS. As in the case of state 1, the following two Laplace transform equations are given by the equivalent circuit of state 3 shown in Fig. 5. The default values of i_{1c} and i_{2c} are set as zero.

$$\frac{V_0}{s} = -r_1 \{I_{1c}(s) + I_{2c}(s)\} - \left(\frac{Ls + r_L}{2} + 2r_T + r_0 \right) I_{2c}(s) - \frac{2v_T}{s} + V_M(s) + \frac{V_1}{s} \quad (11)$$

$$\frac{V_1}{s} = r_1 \{I_{1c}(s) + I_{2c}(s)\} + \left(\frac{Ls + r_L}{2} + 2r_T \right) I_{1c}(s) + V_M(s) \quad (12)$$

Since $i_{1c} = i_{2c}$, (13) is obtained from (11) and (12).

$$I_{1c}(s) = I_{2c}(s) = \frac{2V_1 - V_0 - 2v_T}{Ls \left(s + \frac{r_L + 4r_T + r_0 + 4r_1}{L} \right)} = \frac{V_{1c}}{r_b} - \frac{V_{1c}}{s + \frac{r_b}{L}} \quad (13)$$

Here, (14) is obtained from the following equations.

$$r_b = r_L + 4r_T + r_0 + 4r_1, \quad V_{1c} = 2V_1 - V_0 - 2v_T$$

$$i_{1c}(t) = i_{2c}(t) = \frac{V_{1c}}{r_b} \left(1 - e^{-\frac{r_b t}{L}} \right) \quad (14)$$

Further, when the current is defined as I_1 at time T , (15) is obtained from (14).

$$I_1 = \frac{V_{1c}}{r_b} \left(1 - e^{-\frac{\pi r_b (1-D)}{\omega L}} e^{-\frac{\pi r_b T_2}{\omega L T}} \right) \quad (15)$$

B. Numerical calculations of AC output current waveforms

Using the values of I_1 and I_2 , which are derived from (5), (10) and (15), (16) and (17) can be obtained.

$$I_1 = \frac{\frac{V_{1a}}{r_a} \frac{r_b}{V_{1b}} \left(1 - e^{-\frac{\pi r_a D}{\omega L}} \right) e^{-\frac{\pi r_b (1-D)}{\omega L}} + 1 - e^{-\frac{\pi r_b (1-D)}{\omega L}}}{\frac{r_b}{V_{1c}} + \frac{r_b}{V_{1b}} e^{-\frac{\pi r_a D}{\omega L}} e^{-\frac{\pi r_b (1-D)}{\omega L}}} \quad (16)$$

$$I_2 = \frac{\frac{V_{1a}}{r_a} \frac{r_b}{V_{1c}} \left(1 - e^{-\frac{\pi r_a D}{\omega L}} \right) - \left(1 - e^{-\frac{\pi r_b (1-D)}{\omega L}} \right) e^{-\frac{\pi r_b D}{\omega L}}}{\frac{r_b}{V_{1c}} + \frac{r_b}{V_{1b}} e^{-\frac{\pi r_a D}{\omega L}} e^{-\frac{\pi r_b (1-D)}{\omega L}}} \quad (17)$$

Table 1 Circuit symbols and parameters

FET threshold voltage	v_T	0.2V
FET on-resistance	r_T	100m Ω
Transformer total resistance	r_L	100m Ω
Internal resistance of low-voltage source	r_I	1m Ω
Internal resistance of high-voltage source	r_o	1m Ω
Transformer leakage inductance	L	220 μ H
Transformer voltage	v_M	160V = $V_o/2$
Switching frequency	f	20kHz
DC voltage on low-voltage side	V_I	160V
DC voltage on high-voltage side	V_o	320V

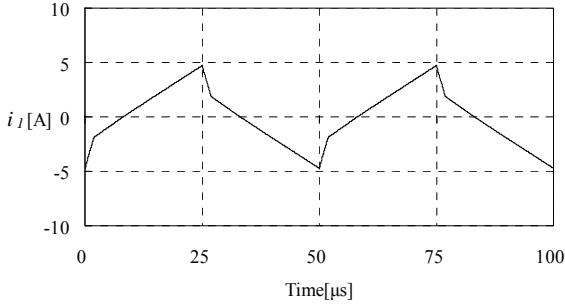


Fig. 7. Transformer primary current (i_I) in pattern (a) in power running mode. (input voltage 192V, output voltage 320V, output power 500W)

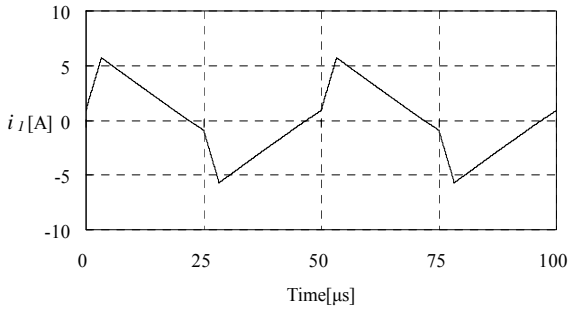


Fig. 8. Transformer primary current (i_I) in pattern (b) in power running mode. (input voltage 128V, output voltage 320V, output power 500W)

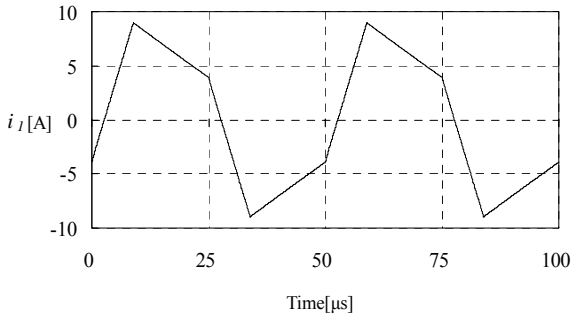


Fig. 9. Transformer primary current (i_I) in pattern (c) in power running mode. (input voltage 128V, output voltage 320V, output power 1kW)

We obtained I_1 and I_2 by substituting parameters listed in Table 1 into (16) and (17). Then, numerical calculations were made using (4), (9) and (14) to obtain transformer primary current (i_I). Fig. 7 shows the waveform in pattern (a) in power running mode. Similar analysis was carried out for patterns (b) and (c), to obtain i_I by changing the value of V_I , as shown in Figs. 8 and 9.

IV. EXPERIMENTAL RESULTS

We constructed a prototype of the proposed DC-DC converter, with the following specifications: rated output capacity $P_o = 1$ kW, rated voltage on low-voltage side $V_I = 160$ V, and rated voltage at high-voltage side $V_o = 320$ V. Using the prototype, its conversion efficiency was evaluated by testing under the control of a feedback-loop system.

A. Conversion efficiency characteristics of proposed DC-DC converter

Fig. 10 shows the conversion efficiency of the proposed DC-DC converter in power running mode in case of use of FET and IGBT. In the test, FET and IGBT with similar rated values were provided by the same manufacturer. Note that power required for control power source is not included in conversion efficiency. FET and IGBT were connected to fast recovery diodes in reverse parallel. Ferrite was used as the core material for the high frequency transformer, which incorporated a mechanism to enfold leakage inductance. As a result of evaluation testing, at the rated input/output voltage with the rated output of 1kW, in the case of FET, conversion efficiencies of 98.2% in power running mode were achieved. In the half load region, 99.1% was obtained in power running mode. In all cases, high conversion efficiency was achieved. We concluded that, except in the case of light load, FET was 1.5% more power efficient than IGBT.

B. Effect of synchronous rectifier

Fig. 11 shows a typical power flow in the case of use of IGBT, and Fig. 12 shows that in the case of use of FET, during power running mode in which power flows from the low-voltage side to the high-voltage side. When using IGBT, the current flowing to converter 2 flows through diodes in an anti-parallel connection with switching elements. So converter 2 provided rectification effect.

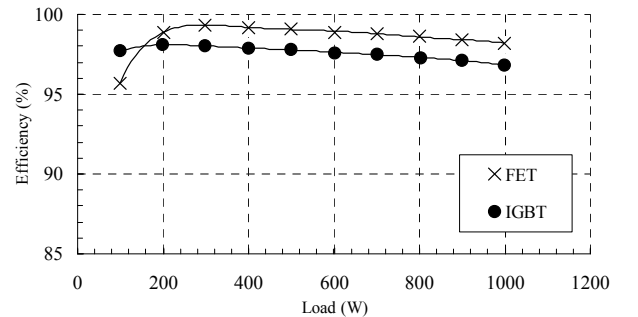


Fig. 10. Conversion efficiency in power running mode.

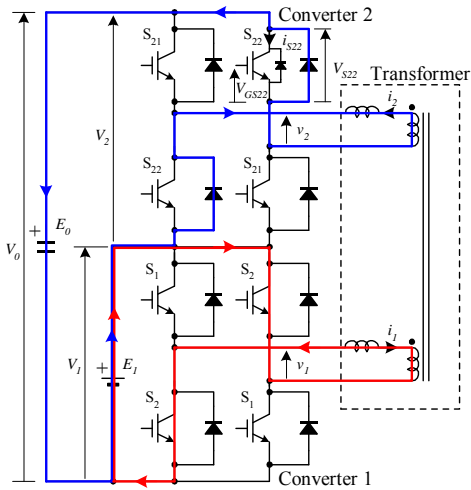


Fig. 11. Power flow in the case of use of IGBT.

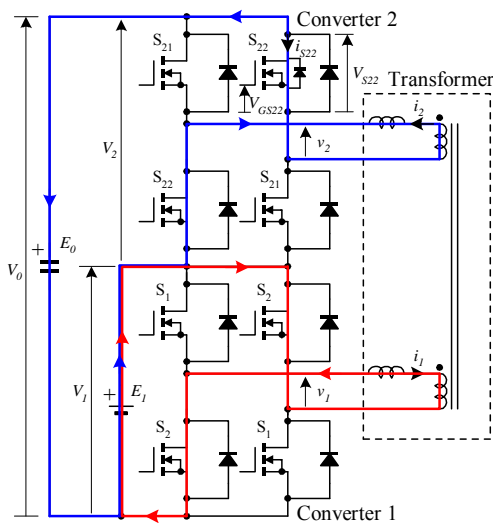


Fig. 12. Power flow in the case of use of FET.

When using FET, the current flowing to converter 2 flows through switching elements. So converter 2 provided synchronous rectification effect. Fig. 13 shows the turn-on voltage waveform of S_{22} when using IGBT, while Fig. 14 shows that when using FET. When using IGBT, the turn-on voltage was approximately 0.9V. It was found that the current flowed through diodes in an anti-parallel connection with S_{22} , not through switching elements, as shown in Fig. 13. In contrast, when using FET, the voltage drop was approximately 0.4V due to the FET drain current, as shown in Fig. 14. This led to the finding that the current flowed through switching elements, not diodes in an anti-parallel connection with S_{22} . That is, a synchronous rectification effect was provided. From the results, it was shown that the turn-on loss was reduced by half when using FET.

V. CONCLUSION

Through the performance analysis and evaluation test, the authors were able to theoretically clarify the behavior of

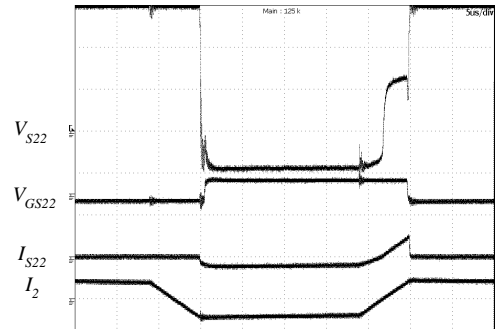


Fig. 13. Turn-on voltage waveform when using IGBT.

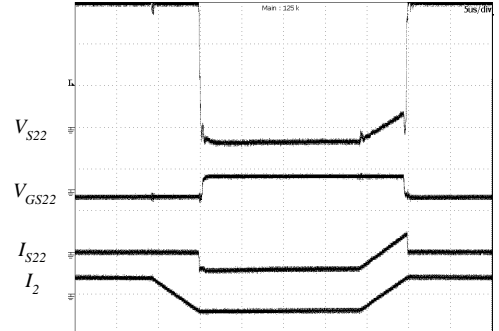


Fig. 14. Turn-on voltage waveform when using FET.

their proposed DC-DC converter and the effect of synchronous rectification function. As a result of evaluation testing, in the case of rated output of 1kW, conversion efficiency of 98.2% in power running mode were achieved. The future approach will be to carry out a detailed analysis of power losses. In addition, further efforts will be made to resolve conversion efficiency drop resulting from the hard-turn-on phenomenon, aimed at the further improvement of efficiency.

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