IEICE TRANS. COMMUN., VOL.E93–B, NO.9 SEPTEMBER 2010

PAPER Special Section on Telecommunication Energy Technology in Conjunction with Main Topics of INTELEC'09

Totem-Pole Power-Factor-Correction Converter under Critical-Conduction-Mode Interleaved Operation*

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SUMMARY This paper proposes a new power-factor-correction (PFC) topology, and explains its operation principle, its control mechanism, related application problems followed by experimental results. In this proposed topology, critical-conduction-mode (CRM) interleaved technique is applied to a bridgeless PFC in order to achieve high efficiency by combining benefits of each topology. This application is targeted toward low to middle power applications that normally employs continuous-conduction-mode boost converter.

key words: *PFC, Interleaved, critical-conduction-mode, totem-pole*

1. Introduction

The interleaved version of critical-conduction-mode (CRM) boost power-factor-correction (PFC) converter is a good alternative to the renowned continuous-conduction-mode (CCM) boost PFC converter. It is composed of bridge diodes ($D_{b1} - D_{b4}$) and two boost converters connected in parallel (Fig. 1) [1].

The CRM operation mode of the converter results in zero-current-switch (ZCS) turn on transition (i_{S1} and i_{D1} of Fig. 2). Moreover, resonance between main switch parasitic capacitance and input inductor gives nearly zero-voltage-switching (ZVS) turn on transition (v_{S1} of Fig. 2). Both conditions make efficiency of the converter very high and less pronounced by boost diode reverse recovery problem [2].

The mentioned topology also makes PFC control scheme simpler. As a first order system, the converter is relatively easy to be stabilized. Other than that, the input current of a constant turn on CRM-boost converter will automatically be proportional to its input voltage. Therefore, a low-bandwidth output voltage regulator is enough to create PFC function based on the topology [3].

However, the input current of an individual CRM-boost PFC converter looks pulsating as shown by i_{L1} and i_{L2} in Fig. 3. This input current waveform needs significant filtering effort in order to conform EMI standard [4]. Interleaving the boost converters may reduce current spikes by producing quasi-continuous input current (i_i in Fig. 3). It is achieved by operating each converter 180° out of phase [4]–[6]. With this kind of input current, EMI filtering will be less demanding [7].

A bridgeless PFC topology is another form of high ef-

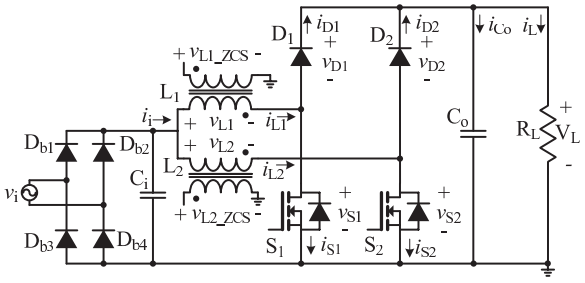

Fig. 1 A conventional CRM-interleaved boost PFC converter.

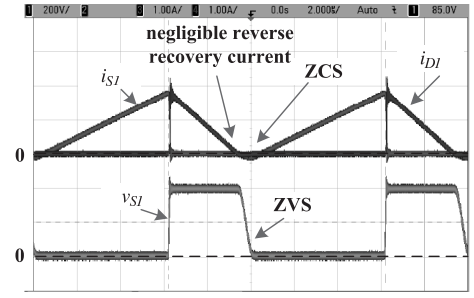

Fig. 2 i_S, i_D, and v_S of a conventional CRM-interleaved boost PFC converter.

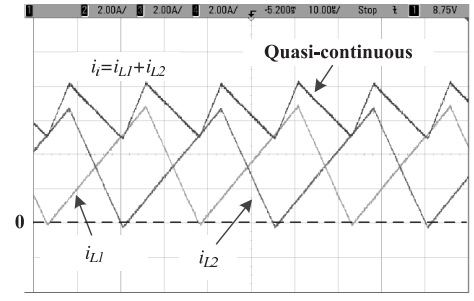

Fig. 3 Input current of a conventional CRM-interleaved boost PFC converter.

Manuscript received January 18, 2010.
Manuscript revised May 10, 2010.

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*This paper was presented at The International Telecommunications Energy Conference (INTELEC) 2009.

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DOI: 10.1587/transcom.E93.B.2250

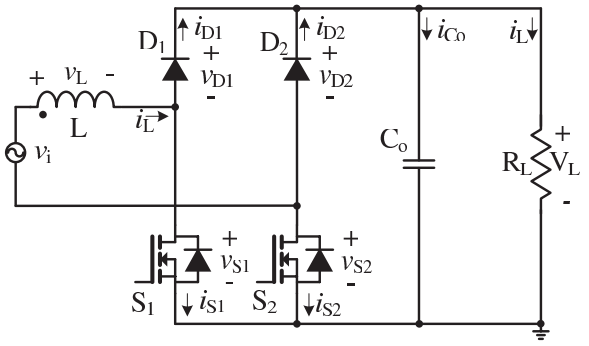


Fig. 4 Basic bridgeless PFC topology [8].

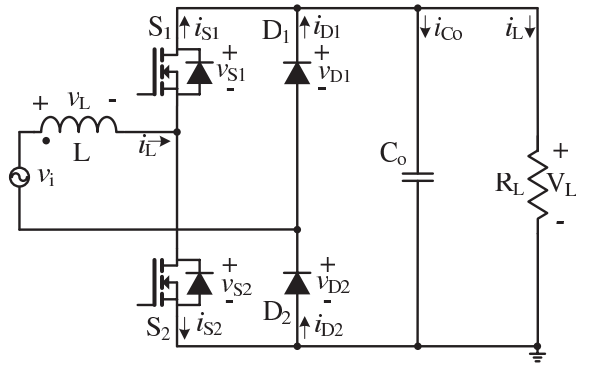


Fig. 5 Totem-pole dual-boost PFC rectifier [9].

ficient converter. It also consists of two boost converters as formerly mentioned in the CRM-interleaved boost PFC topology. However, they are connected in serial instead of parallel (Fig. 4 and Fig. 5) [8], [9].

High efficiency character of this converter is achieved by excluding bridge diodes from the PFC circuit. As a consequence, one series diode voltage drop can be saved. Theoretically, it may reclaim about 1% of conduction loss [10].

In this paper, a new bridgeless-PFC topology is proposed. The new topology works under CRM-interleaved scheme. The proposed converter gives least component and simplest circuitry compared to other possible combination of CRM-interleaved and bridgeless topology. Ideally, the absence of the bridge diodes in this PFC circuit makes its efficiency even higher compared to conventional CRM-interleaved boost PFC topology. Further details regarding schematic circuit, operation principle, equations, control mechanism, related application problems, and experimental results will be explained in the later part of this paper.

2. Basic Building Blocks

2.1 Problems with the Basic Bridgeless Boost PFC Topology

Circuit in Fig. 4 has larger common-mode conducted noise than conventional boost PFC topology [11]. Therefore, the circuit is impractical to recent strict noise regulation.

Moreover, interleaving a basic bridgeless PFC topology results in four boost converters: two in series to form a bridgeless PFC converter; multiplied by two to form interleaved function. It needs four switches, four diodes, and two to four inductors (depend on topology selection). Those are quite numerous numbers of semiconductors.

2.2 The Totem-Pole Bridgeless Topology

An interesting topology called totem-pole dual-boost PFC topology is presented in Fig. 5 [9]. This circuit is less suffer from high common-mode noise problem [12]. Moreover, when the topology is operated under interleaved scheme, it needs fewer components compared to the one based on the circuit in Fig. 4.

The totem-pole topology uses body diode of the MOSFET as its catch diode. Normally, this kind of diode has long reverse recovery time. This fact suggests that the referred circuit is only suitable for DCM (discontinuous conduction mode) and CRM operation [11].

Fortunately, this limitation does not affect too much to this research. Because, the basic circuit of CRM-interleaved topology is of course intended to work under critical-conduction-mode. With the advantage of less components requirement, this topology becomes a good candidate to be the basic topology.

3. The Proposed Topology

3.1 Detailed Circuit

Figure 6 shows schematic diagram of the proposed converter [13]. It is basically similar to the circuit of Fig. 5 with additional inductor (L_2) and extra switch-leg (S_3 and S_4) to implement interleave function.

As the proposed circuit is intended to work under CRM operation, its inductors structure (L_1 and L_2) are similar to the one in Fig. 1. They are equipped with secondary winding to detect i_{L1} and i_{L2} zero-current instance.

3.2 Operation Principle

Related to bridgeless operation, switches in Fig. 6 can be grouped into positive-phase group (S_2 and S_4) and negative-phase group (S_1 and S_3). The positive-phase group operates as boost-switches during positive phase of v_i. At this period, body-diodes of the negative-phase group work as the catch diode and return current is delivered by D_2. The converter operation during this stage is illustrated by Fig. 7(a).

When v_i is in its negative phase, the opposite condition occurs. Through out this time, negative-phase group operates as the boost switches and the catch diodes are served by the body diodes of positive-phase group. Return current is handled by D_1. Figure 7(b) depicts this condition.

Regarding the interleaved function, converter in Fig. 6 can be divided into two full functional converters. Converter 1 consists of L_1, S_1, and S_2 while converter 2 consists of L_2,

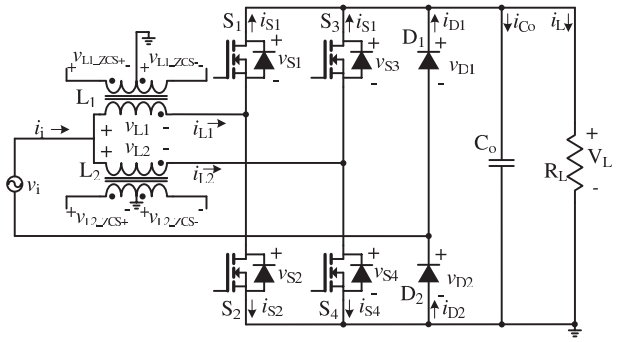
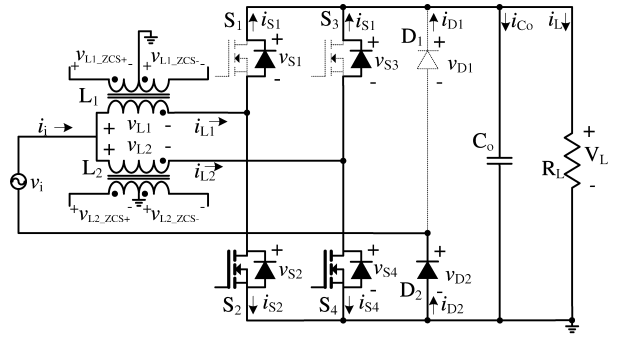
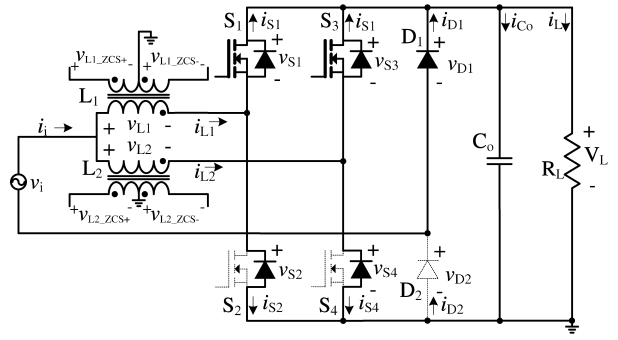


Fig. 6 The proposed converter.



(a) During positive phase of v_i.



(b) During negative phase of v_i.

Fig. 7 Switch configuration of the proposed converter related to the phase of v_i.

S_3, and S_4.

Interleaved control function will make sure operation of converter 1 is 180° out of phase to converter 2 in order to maximize the input current ripple cancellation. However, technique to achieve optimum interleave function is outside the scope of this paper. References [14] and [15] discuss further options related to this matter.

3.3 Control Scheme

Figure 8 shows the control block diagram for the proposed converter [16]. Its main part is similar to the conventional CRM-interleaved boost PFC topology. Therefore, commercially available controller for that kind of converter can be used as the core controller. However, to accommodate bridgeless nature of the proposed converter, three additional

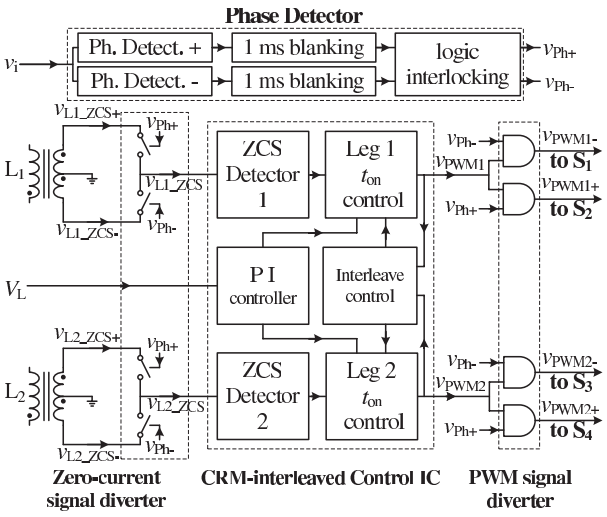


Fig. 8 Control scheme of the proposed converter.

circuits were added.

3.3.1 Phase Detector

A phase detector unit monitors the state of v_i. It produces two phase detection signals; v_{Ph+} and v_{Ph-}. v_{Ph+} generates logic high during positive phase of v_i, otherwise it produces logic zero. When v_i is under negative phase, v_{Ph-} produce logic high. It will be zero during all other conditions.

Those two signals are generated by two independent, interlocked, and edge-blanked detection circuit to avoid phase detection mistake around v_i zero-crossing instance. Two independent phase detection circuitry were selected in order to generate symmetrical signals among v_{Ph+} and v_{Ph-} while still accommodating slight inaccuracy in the real circuit operation. The logic interlocking mechanism avoids v_{Ph+} and v_{Ph-} to generate logic high in the same period. While, edge-blanking circuit keeps the logic stable even though oscillation occurs after v_i zero-crossing period.

3.3.2 Zero-Current Signal Diverter

The CRM-interleaved boost PFC controller needs to monitor the zero-current instant time of i_{L1} and i_{L2} to determine the next switching cycle. The circuit responsible to this control function needs particular logic transition to fulfill its operation.

In order to minimize conduction loss and component cost, the detector does not incorporate resistor sensing technique or current transformer. Instead, it is implemented as secondary winding of the boost inductors [17], [18]. Voltage relation between primary winding and secondary winding can be determined as,

$$v_{L_S} = \frac{n_s}{n_p} \times v_{L_P}. \tag{1}$$

Where, v_{L_P} and v_{L_S} are the voltage over primary and secondary winding while, n_p and n_s are number of primary and

secondary turns respectively.

Inductors of the conventional CRM-interleaved boost PFC topology is located in DC side. Therefore, the polarity v_{L1} and v_{L2} of Fig. 1 are constant. It makes the output of its secondary winding (v_{L1_ZCS} and v_{L2_ZCS} of Fig. 1) meet to the PFC controller logic requirement. Therefore, they can be directly connected to the controller.

However, input inductors of the proposed converter are now located in the AC side. As the consequence, phase of v_{L1} and v_{L2} of Fig. 6 alternate each time v_i changes its polarity (Fig. 9). Two modifications are required to connect the output of L_1 and L_2 secondary winding to the controller [16],

- implement the detection winding as center-tapped winding,
- adding a zero-current signal diverter.

The center-tapped winding modification make each inductor generate complementary zero-current signals. The zero-current signal diverter selects which signal should be connected to the ZCS-detector of the main controller according to v_{Ph+} and v_{Ph-} logic condition. When v_{Ph+} gives logic high, v_{L1_ZCS+} and v_{L2_ZCS+} are connected to the main controller. In the other side, if v_{Ph-} gives logic high, v_{L1_ZCS-} and v_{L2_ZCS-} are the one who should be connected to the main controller. The resulting waveforms of this circuit are labeled v_{L1_ZCS} and v_{L2_ZCS} (Fig. 8). The similar name of the referred waveforms to those of conventional CRM-interleaved boost PFC converter indicates characteristics similarity among them.

3.3.3 PWM Signal Diverter

Stated in Sect. 3.2 that proposed converter consists of positive and negative switch groups. The switch groups should be driven synchronously to the phase detection signal.

Accommodating this distinct character of the proposed converter, a PWM signal diverter is added. With this diverter, PWM signals are directed to positive-phase group (S_2 and S_4) when v_{Ph+} is high. Otherwise, the signals will be sent to negative-phase group (S_1 and S_3) when v_{Ph-} is high.

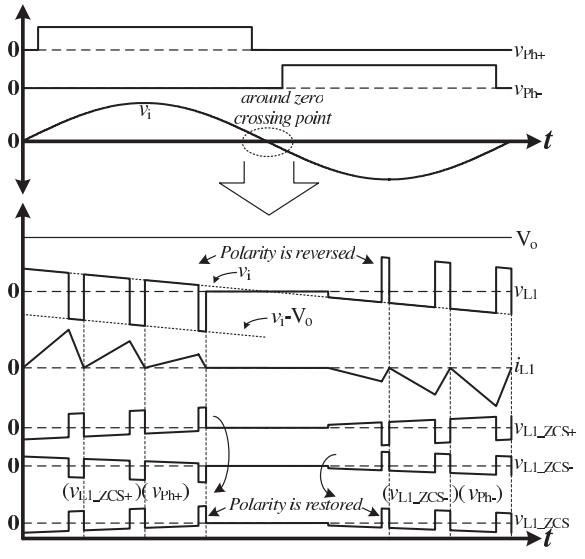


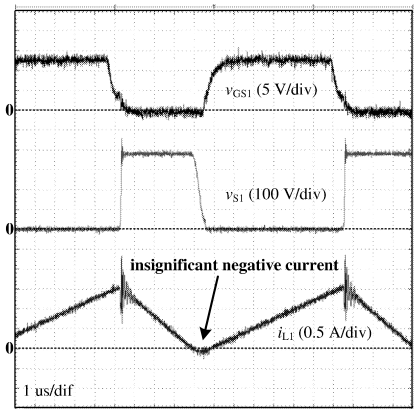
Fig. 9 Illustration of voltage waveforms generated by inductor's sense winding inside the proposed converter.

4. Practical Problems

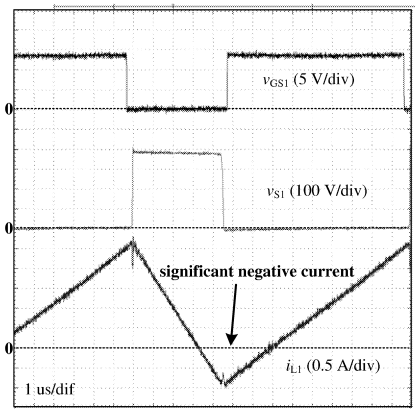
4.1 Reverse Recovery Current of Body Diodes

The proposed converter utilizes MOSFET's body diodes to be used as catch diode. It should be note that body diode characteristics are not as good as a well-designed diode. This diode is actually side effect intrinsic to the MOSFET structure and is common to have ten times or more recovery charge compared to a fast recovery diode.

The higher recovery charge of the body diode makes i_{L1} of the proposed converter has significant negative current (Fig. 10(b)). This condition is not occurred in a conventional CRM-interleaved boost PFC topology (Fig. 10(a)). The negative current gives penalty toward converter efficiency as illustrated later in Fig. 13(a) of Sect. 5.



(a) Conventional CRM-interleaved boost PFC converter.



(b) The proposed converter.

Fig. 10 Comparison of i_{GS}, v_{DS}, and i_L in the conventional CRM-interleaved boost PFC converter to the proposed converter.

4.2 Voltage Ringing Near v_i Zero-Crossing

Every time v_i crossing the zero-point heading to a new phase, the proposed converter enters an idle condition. Its waveforms during idle and some period after that is shown in Fig. 11. The parasitic capacitance condition during (−) to (+) phase transition is shown in Fig. 12 with:

- C_{Sn} is parasitic capacitance of S_n; n=1,2,3,4;
- C_{Di} is parasitic capacitance of D_i; i=1,2;
- C_{Bj} is parasitic capacitance of the switch legs; j=1,2,3.

Careful attention should be made on those parasitic capacitances. With condition as stated in Fig. 12, C_{D2} will be discharged through L_1 and v_i on the first PWM signal. Here, discharging process occurs under resonant condition of L_1 and all other parasitic capacitances.

It should be noted that at this moment, v_i is still very small and is in phase to the charge stored inside C_{D2}. This creates current pulse and excites quite disturbing voltage and current oscillation as shown in Fig. 11.

The oscillation occurs in two different areas:

- C_{Sn}, C_{Di}, and L_1 generate oscillation reverenced to the neutral point,
- C_{Bj} and L_1 generate oscillation reverenced to the earth.

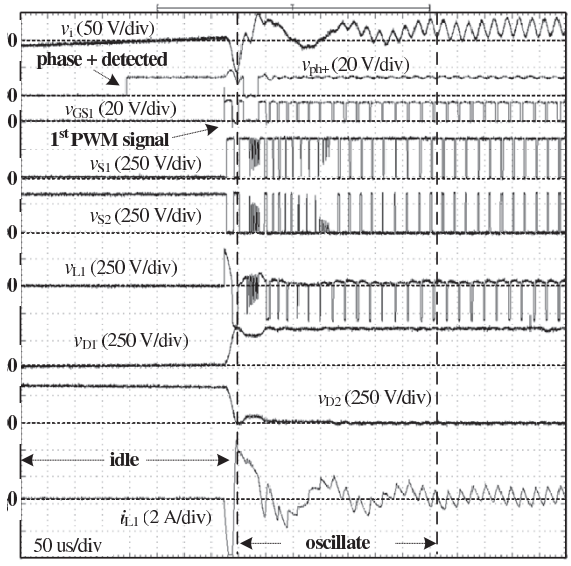


Fig. 11 The proposed topology key-waveforms during phase transition.

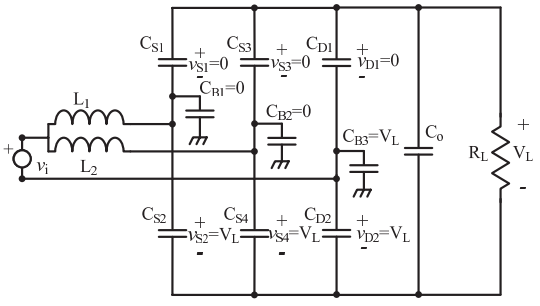


Fig. 12 Parasitic capacitaces in the proposed circuit during v_i phase transition from − to +.

The voltage and currents oscillation result in several problems like:

- The phase detector circuit generates wrong phase detection signal. This condition may result in catastrophic event.
- Oscillation occurs among L_1, C_{Sn}, and C_{Di} increase differential-mode conduction noise.
- Oscillation between L_1 and C_{Bj} increase common-mode conduction noise.

Therefore, voltage and current ringing near zero-crossing-point of v_i should be addressed properly in order to achieve good performance of the proposed converter.

5. Experimental Results

Breadboards have been built as three prototypes of the proposed converter and two types of conventional CRM-interleaved boost PFC converters. Those two types of the conventional CRM-interleaved boost topology were used to find out the effect of body-diode usage on the converter efficiency. Specifications of the converters are listed in Table 1.

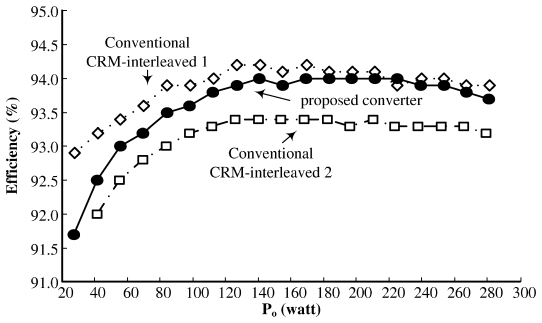
Theoretically, an ideal diode will not affect the efficiency of an CRM-interleaved boost PFC converter. However, the actual circuit measurement reveals that the conventional CRM-interleaved 2, which uses body diodes as its catch diode, has the effect of efficiency decrease as shown in Fig. 13(a).

In the same figure, it can be seen that the peak efficiency of the proposed converter is about 1% higher than the conventional CRM-interleaved boost type 2. This is close to efficiency improvement estimation stated in [10]. However, the proposed converter still cannot outperform the conventional CRM-interleaved boost type 1 which uses the ultra-fast recovery diodes. The reason for this matter is due to the diode recovery characteristics as explained in Sect. 4.1.

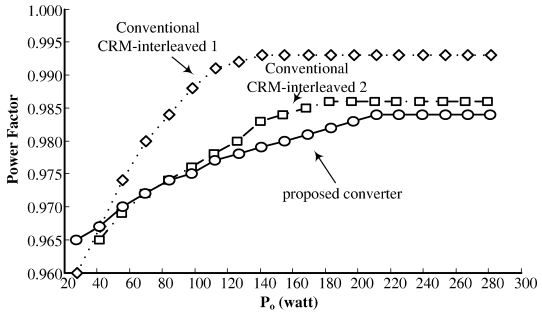
Concerning the power-factor, three-type converters have prominent features higher than 0.96 as shown in Fig. 13(b), though the proposed one is not superior to the conventional one. Figure 14 shows that the input-current harmonic components in the proposed converter was sufficiently suppressed and complied with IEC61000-3-2 Class D limitation.

Table 1 Parameter list of the converters.

	Proposed Converter	Conventional CRM-interleaved 1	Conventional CRM-interleaved 2
P_{o_max}	300 W	300 W	300 W
S_1 - S_4	SPP11N60CFD	SPP11N60CFD	SPP11N60CFD
D_{b1} & D_{b4}	-	RBV404	RBV404
D_1 & D_2	MURS360T3	MURS360T3	Body-diode of SPP11N60CFD
L_1 & L_2	370 μH	370 μH	370 μH
C_o	200 μF	200 μF	200 μF
V_o	360 V	360 V	360 V



(a) Efficiency characteristics.



(b) Power-factor characteristics.

Fig. 13 Efficiency and power-factor characteristics of the proposed topology compared to the conventional CRM-interleaved boost PFC converter.

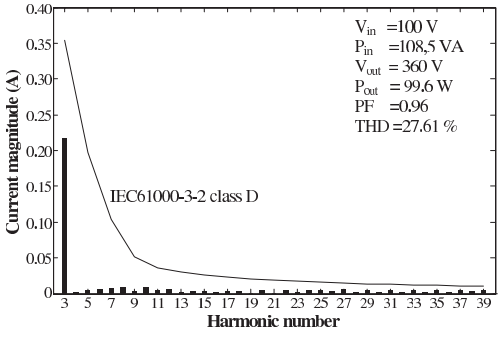


Fig. 14 i_i harmonic measurement of the proposed converter.

Figure 15 describes about current condition inside i_{L1} and i_i. It is clear that even though i_{L1} contains fast change current signal, it becomes smoother while combined with the i_{L2} and results for i_i. This is the merit of an interleaved boost technique.

6. Conclusions

A bridgeless CRM-interleaved boost PFC converter based on totem-pole topology has been presented. Its basic principle, detailed control scheme, implementation problems, and experimental results have been shown thoroughly. It is evident that the new topology, at recent stage, be able to pass the IEC61000-3-2 class D standard while also performing reasonable efficiency even though some practical problems are still exist. Further developments toward better results are still widely open and promising. This new topology is a good candidate toward low to middle power PFC converter.

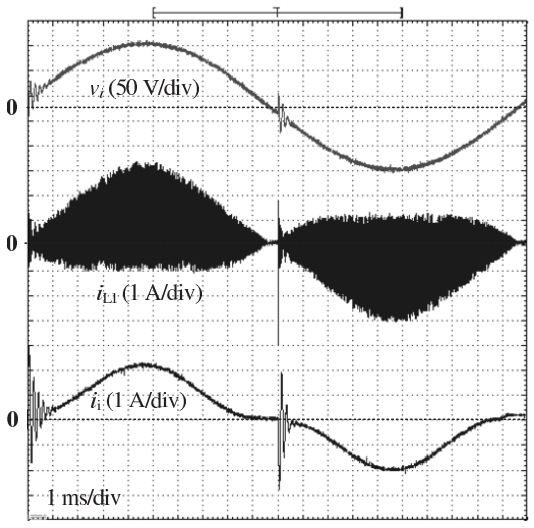


Fig. 15 v_i, i_{L1} and i_i waveform of the proposed converter.

7. Future Work

Further improvement of the proposed converter efficiency is important. Latest IGBT technology can be a good candidate in replacing traditional MOSFET in this area. The new generation IGBT is able to work near hundreds kilohertz switching frequency region, furthermore it does not have body diode problem of MOSFET.

Input voltage and current glitch near zero-crossing should also be addressed properly. The glitch may also give some penalties to the efficiency of the converter.

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