A Design for Small Time-Delay Control Circuit for DPWM- POL

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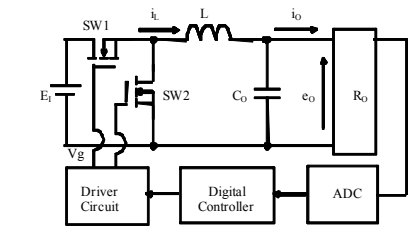
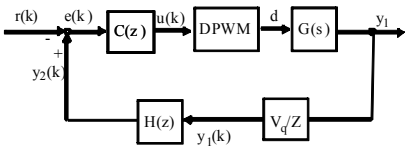
Abstract— **Digital-controlled switching mode power supplies (SMPS) are popular in the fields of relatively large power supply system. The digital controller is consisted of DSPs or microprocessors performing with software. By contrast, such as on-board SMPSs, adapting digital controller isn't still popular because of its cost or response characteristics even if the controllers are constructed by FPGA or custom LSI which is hardware-logic base. This paper will discuss about the proposed hardware logic type digital controller for on-board SMPS, which is very simple and unique design. And, accuracy improved output voltage detection method for the proposed digital controller is proposed. The some experiments are done. And the results show the validity of the proposed circuits.**

I. INTRODUCTION

Digital electronic products have been spreading quickly by the advancement of the integrations technologies. ICs, DSPs and FPGAs requires a high performance and a high speed due to the trend. Along with the situations, their power consumption are increasing. To suppress the power consumption, the power supply voltage is getting lower toward to sub 1V. Because of the severe voltage margin by the lower power supply voltages, special SMPS, point of load (POL) is disposed very near to the load. The requirements of POL are relative low output voltage with large output current, high load change response, high-efficiency, low cost and etc... Also, the control circuit of POL is required to be high accurate, high speed, adaptive and low cost. We had proposed hardware-logic based digital PWM control circuit is effective to such requirements [1-3]. In this paper, the proposed DPWM control method's principles of operation and circuit configurations are described firstly. At the next, a piecewise linear output voltage detection method is proposed and discussed which can improve the output voltage detection accuracy. Finally, the proposed technique is confirmed with some experiments.



(a) Circuit configuration



(b)Control block

Fig. 1 General DPWM-POL

II. DPWM CONTROL METHOD FOR POL (DPWM-POL)

The circuit configuration of general DPWM controller for POL

The circuit configuration of general DPWM controller for POL is shown in Fig. 1[4-11]. This topology has two major time-delay problems. First, time-delay occurs at A/D converter with the conversion-delay. And, the calculation time of digital controller is another problem. Both of the time-delay directly effects on the response speed of the control circuit and influences stability of the control.

A. The circuit configuration of the proposed DPWM-POL

Figure 2 shows the main and the control circuit configuration of the proposed DPWM-POL in this research. Main POL circuit is a quite ordinary non-isolated buck converter. The control circuit is composed with D/A converter, analog comparator, digital controller and drive circuit.

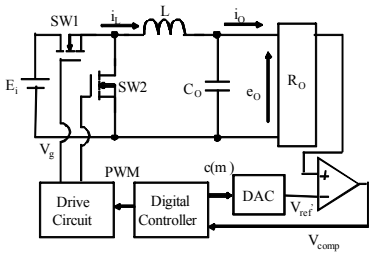


Fig. 2 Circuit configuration of the proposed DPWM-POL

B. The control circuit configuration of the proposed DPWM-POL

Figure 3 shows the control circuit configuration of the proposed DPWM-POL. All blocks are synchronized with the system clock f_{CLK}. Memory1 can store waveform values not only triangle or saw tooth but any waveforms. The output voltage e_o of POL is compared with the converted voltage of memory1's output in the ATC block, successively. The comparator's output is read out to the latch signal to the latch register at the timing that of e_o was sensed. And this latch signal is transferred to DPWM output block. And this latch signal is transfer to DPWM output block.

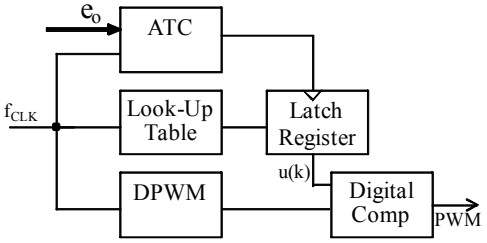
Also, the look-up table method is used for the duty ratio calculation with memory2, 3 and 4. Especially, the duty ratio information which is pre-calculated is stored corresponding to e_o, respectively, in memory2. The duty ratio information is read out from memory2 according to f_{CLK}. At the timing of e_o sensed, one of the duty ratio information is chosen in DFF_4. And the information becomes $u(k)$, where k is the switching term. At the digital comparator, $u(k)$ is converted to real-time analog PWM waveforms. These precise operation technique is described in [2,3]. Fig. 4 shows the waveform of V'_{ref} and V_{comp}.

As a result, comparing with a general digital control method, this proposed control technique doesn't need to calculate the duty ratio information in every switching term, and also the conversion time-delay at A/D converter doesn't exist. Therefore, time-delay drastically decreased to just the sum of calling and the loading time of thememory2.

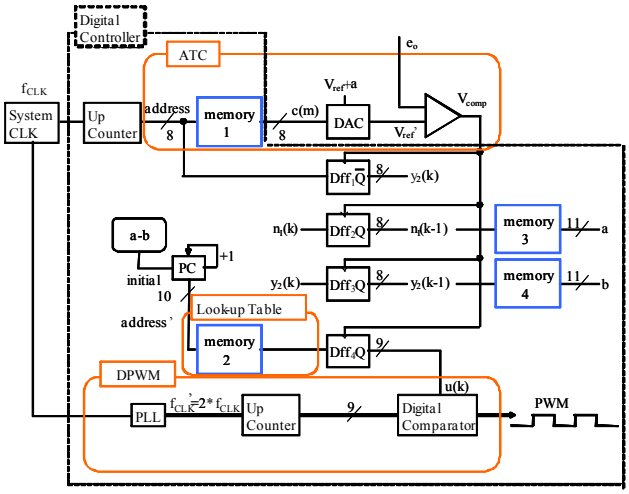
C. Piecewise Linear Output Voltage Detection Method (PLOVDM)

This controller can add the improvement in each block respectively. In this paper, the improvement of the output voltage detection accuracy in the ATC block without any cost-up is aimed. D/A converter used in the ATC block assumes the ladder type, and the output voltage V'_{ref} is provided between two potential of $V^+_{ref}=V_{ref}+\alpha$ and V^-_{ref}:

$$V'_{ref} = \frac{c(m)}{2^n}(V^+_{ref} - V^-_{ref}) + V^-_{ref} \qquad (2.1)$$



(a) Proposed control circuit blocks



(b) Design descriptions of the control circuit blocks

Fig. 3 The system configuration of the part of the proposed control circuit

where $c(m)$ is waveform digital data prestored in memory1, m is clock timing and n is a number of bits. In this time, almost $n+1$ bits accuracy can be achieved by setting as $V_{ref}=V_{ref}/2$ in the n bits system. The detection time will be delay and it will be the trade-off between the accuracy and the time-delay. Therefore, another compensation technique is proposed to solve the trade-off problem. Thanks to the compensation technique, the trade off problem was solved. Precise descriptions will be revealed in proceeding.

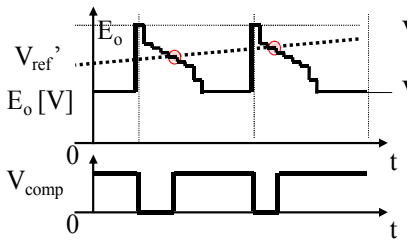


Fig. 4 The waveform of V'_{ref} and V_{comp}

III. EXPERIMENTS

We have done some experiments with the experiment parameters shown in Table 1. The control parameters can be easily modified by rewriting information in memory2. Fig. 5 shows the experimental waveforms. Fig. 6 shows I_O-E_O characteristics. It shows the deviation becomes within 5% in the range of the load change when the proportion gain K_P was larger than 3. Fig. 7 shows E_I-E_O characteristics, where K_P is over 5. The deviation becomes within 10%. Max power efficiency is about 91% shown in Fig. 8. Fig. 9 and Fig. 10 shows dynamic characteristic, where the load change between 0.5A and 5A with 10A/μs slew rate condition, respectively. The mixed-signal oscilloscope Textronix MSO4034 is used to measure analog and digital signal, simultaneously. Blue and Red line shows the output voltage and the output current, respectively. The 9 bits pulse waveforms shown at the bottom of Fig.9 are calculated DPWM of FPGA. Fig. 9 shows the sudden load current increasing result. From this result, after the 1μs voltage drop, the output voltage immediately recovers to the reference voltage. Fig. 10 shows the sudden load current decreasing result. From this result, after the 1μs voltage rising, the output voltage immediately recovers to the reference voltage.

Table. 1 Experiment parameters

Input voltage E_I	3-8V
Output reference V_{ref}	1.5V
Output current I_O	0-6A
Switching frequency f_S	130kHz
Choke inductor L	10μH
Output capacitor C_O	470μF
Proportion gain K_P	1,3,5,7,9
$V_{ref}+\alpha$	1.7V
$V_{ref}-$	0.75V
system CLK f_{CLK}	33.3MHz

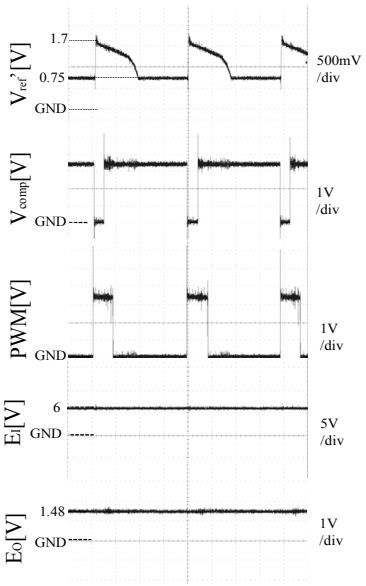


Fig. 5 Experimental waveforms

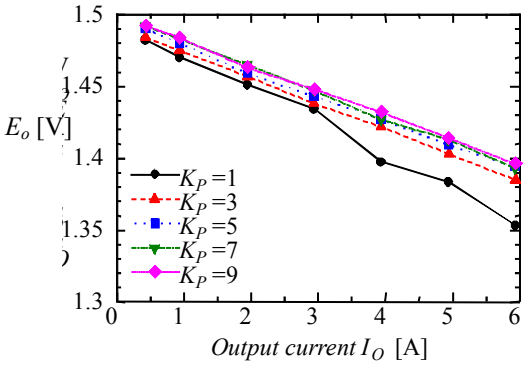


Fig. 6 I_O-E_O Characteristics

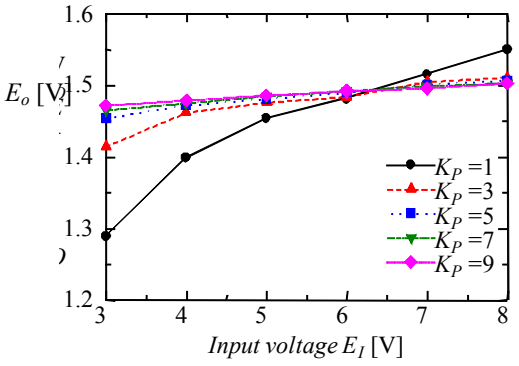


Fig. 7 E_I-E_O Characteristics

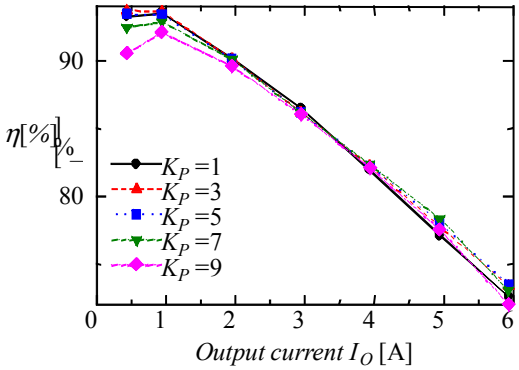
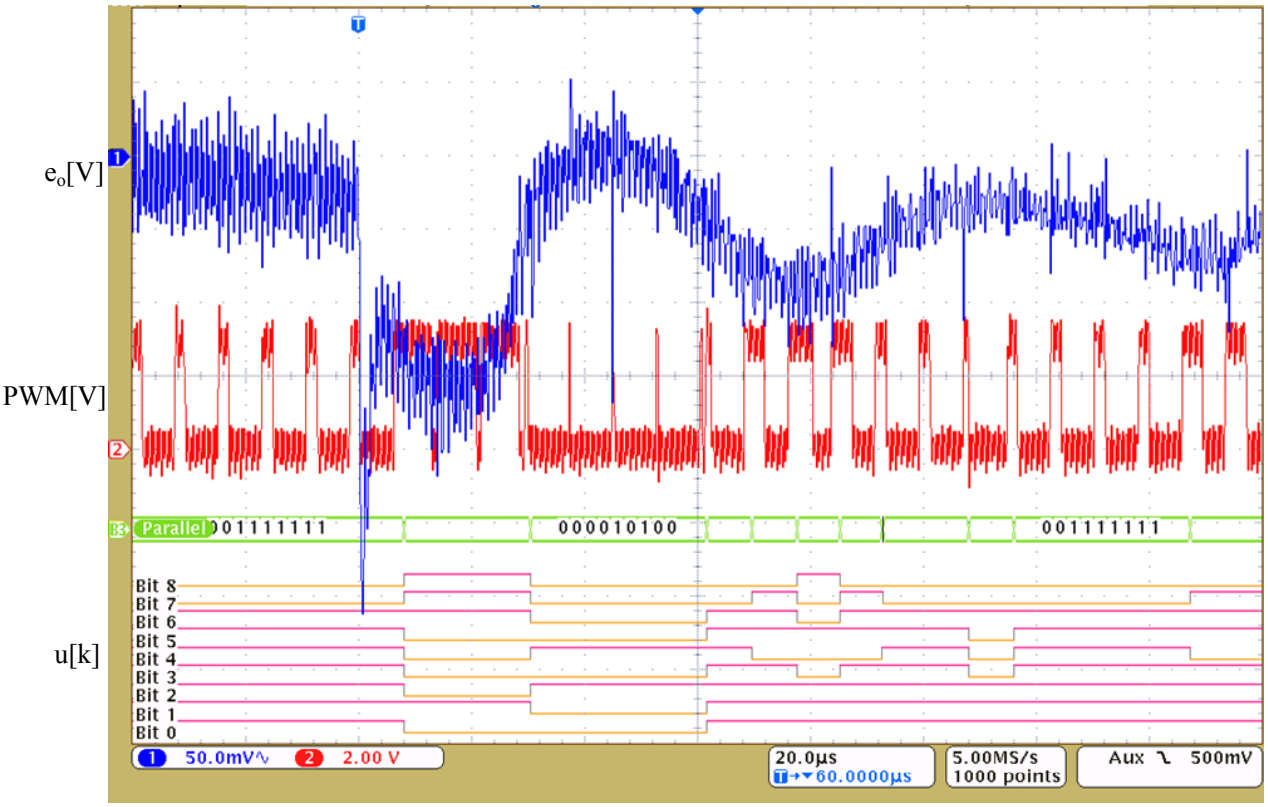


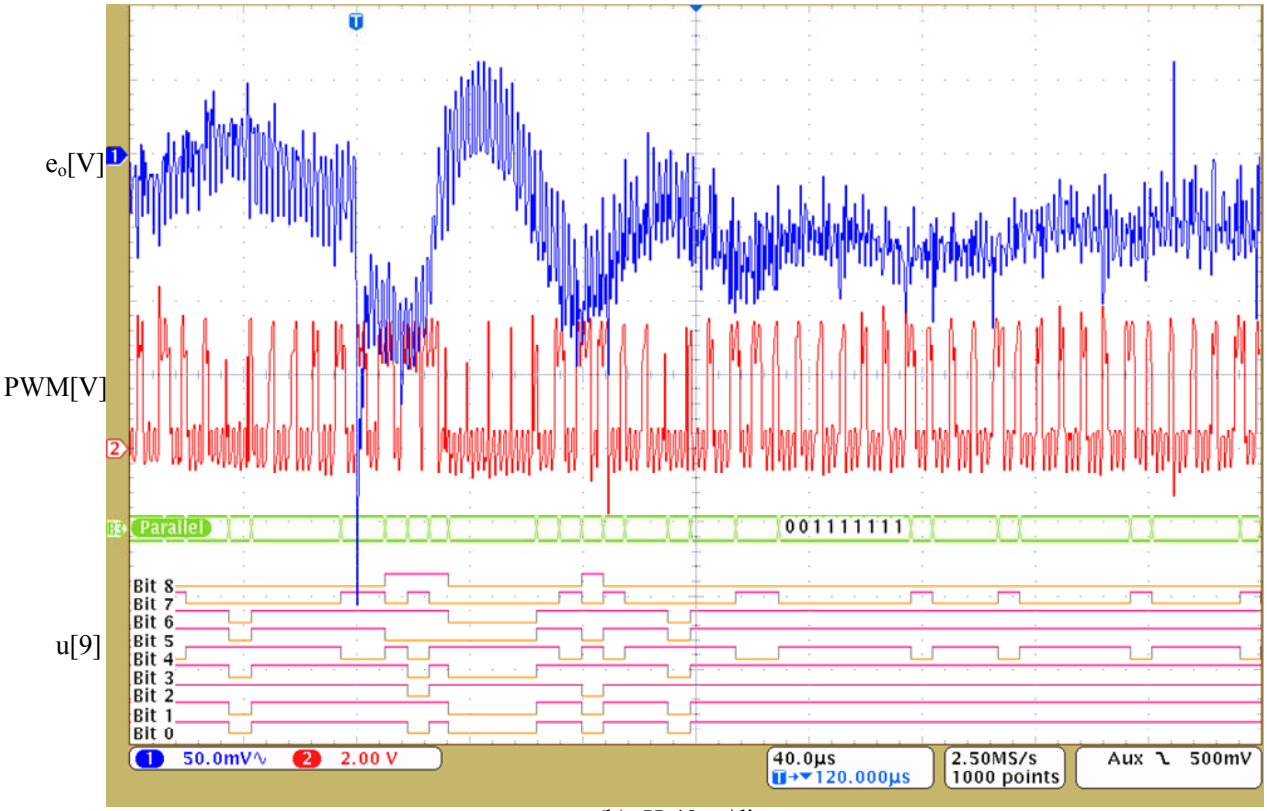
Fig. 8 I_O-η Characteristics

IV. SUMMARY

In this paper, the piecewise linear output voltage detection method for the proposed DPWM-POL is proposed. From the experiment results, it was confirmed that a comparatively steady control was possible by improving the detection accuracy not to accompany the time-delay.

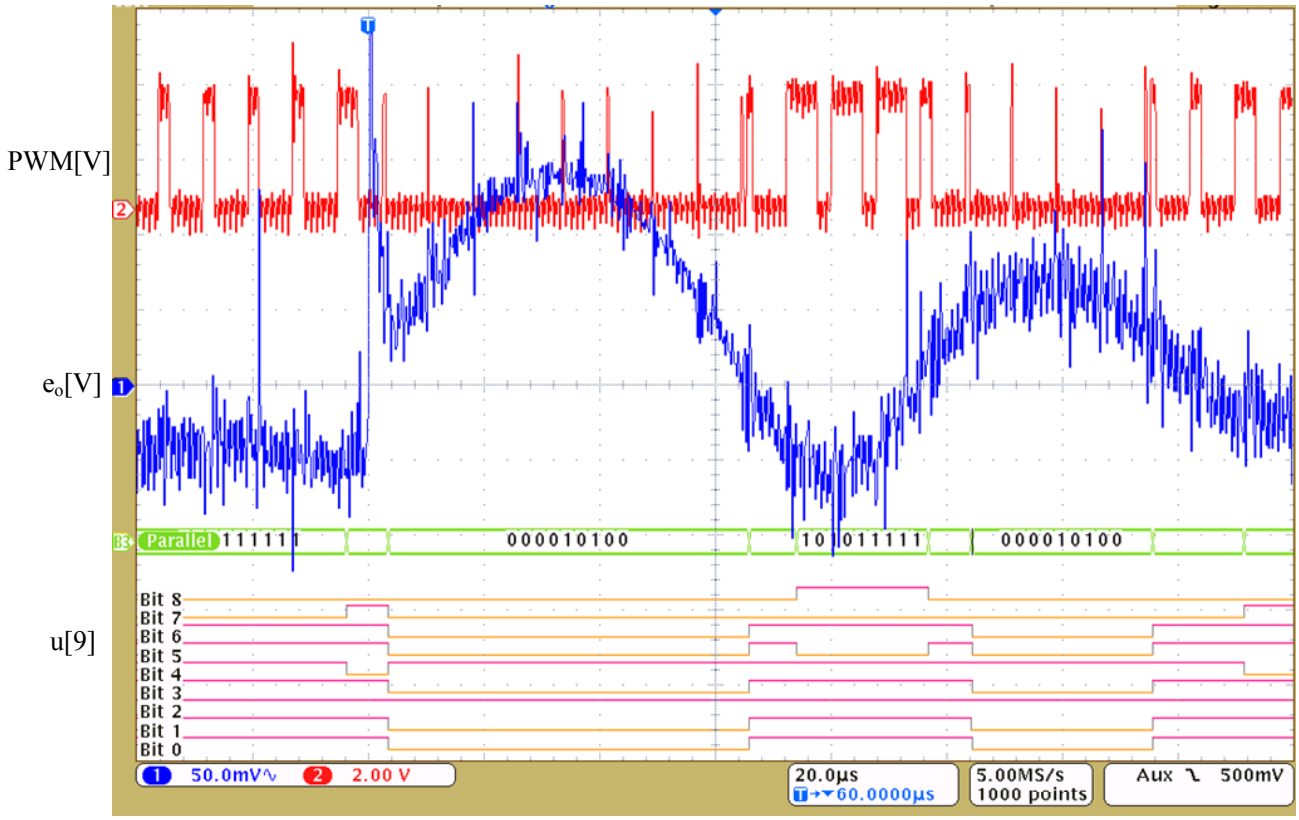


(a) H:20µs/div.

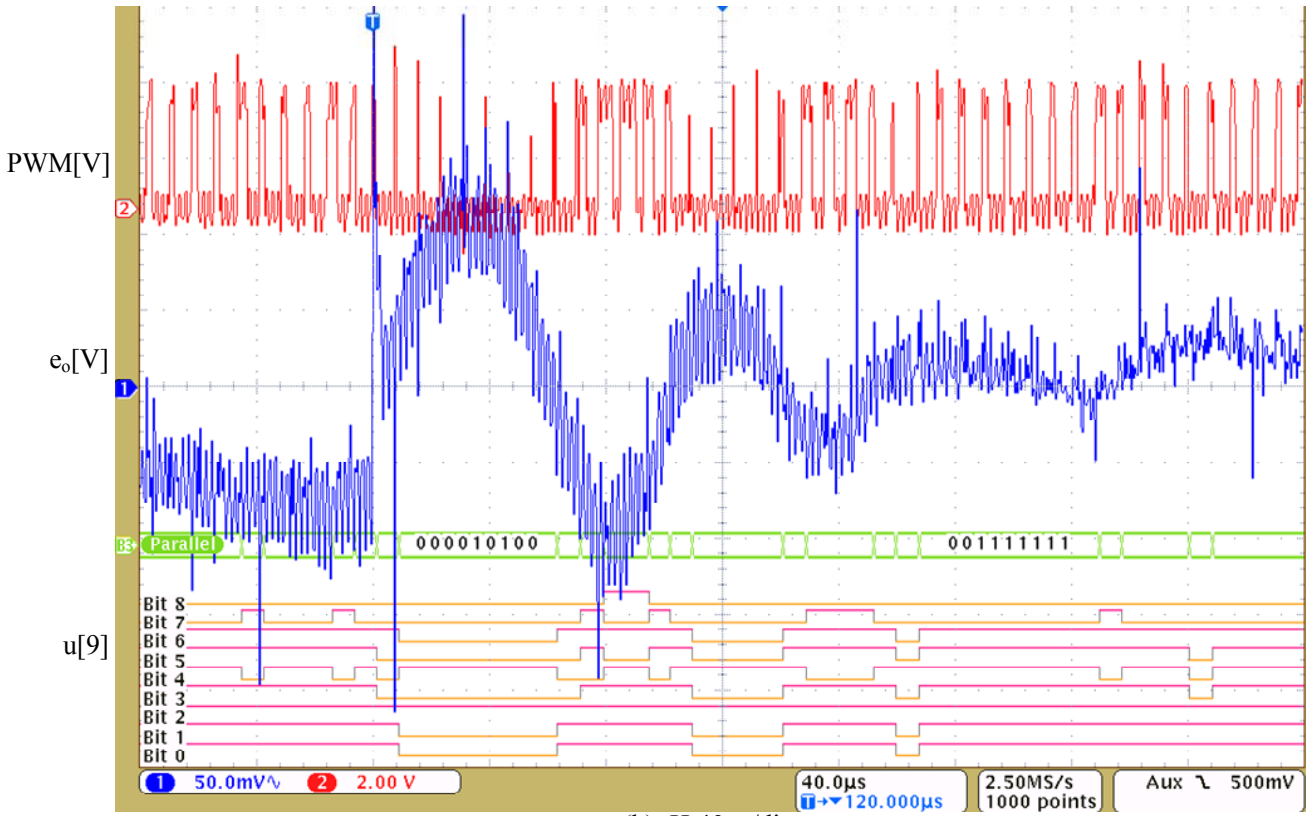


(b) H:40µs/div.

Fig. 9 Dynamic characteristics (from 0.5A to 5A)



(a) H:20µs/div.



(b) H:40µs/div.

Fig.10 Dynamic characteristics (from 5A to 0.5A)

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