Control and PWM Modulation Scheme for Dead-Time Compensation of CVCF Inverters

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Abstract — The switching dead-time necessary in PWM inverters results in output distortions, and deteriorates the utilization of dc-link voltage. To solve these problems, the authors have developed an accurate dead-time effect mathematical model, and proposed a compensation scheme for grid-connected inverters. In this paper, a new voltage control and PWM modulation scheme is presented for the dead-time compensation of CVCF inverters. It consists of a PID voltage controller and a sliding mode controller (SMC). The PID controller operates in the linear areas; the SMC controller detects the dead-time nonlinear operations and operates for the dead-time compensation. In this control scheme, the PWM modulation gate drive is divided into three operation modes according to the SMC controller output. The unnecessary gate drive signals are removed and the counter side switch can be controlled up to truly 100% PWM duty ratio with a smooth transition between different modulation modes. The influence of switching dead-time can be eliminated almost completely.

The proposed control scheme is verified by simulation results. The improvement of harmonic distortion, the minimization of dc-link voltage and the reduction of inductor ripple current are all confirmed by the simulation results. The comparison results between the conventional and the proposed control scheme are presented in this paper.

I. INTRODUCTION

DC/AC inverters are widely used in the telecommunication and data communication systems. Besides the power quality, low cost, small size and high efficiency are the major issues in the power inverters. To address these issues, the industry prefers a higher switching frequency and smaller passive components such as capacitor and inductor.

The dead-time necessary in PWM inverters results in output distortions, and deteriorates the utilization of dc-link voltage. To acquire the desired power quality, a higher dc-link voltage is required, that results in large switching losses [1] and large ripple current. Due to the large inductor ripple current and the high operation voltage of dc-link capacitor, the inductor iron loss increases and a larger dc-link capacitor is required. That will result in large size and high cost. The minimization of dc-link voltage will improve the conversion efficiency and contribute to a reduced size.

For high power quality solutions of power inverters, various control strategies have been investigated for dead-time compensation [2], [3]. Usually the compensation techniques are based on the current polarity. But in the case when a small inductor is used in the LC filter, because of the influence of switching ripple current, it may malfunction and worsen the power quality on the contrary.

To solve these problems, a new voltage control and PWM modulation scheme is proposed in this paper. The proposed controller consists of a sliding controller (SMC) and a PID voltage controller. The PID controller is active when the inverter operates in linear areas. When the dead-time nonlinear operations are detected, the SMC controller operates for the dead-time compensation. According to the SMC controller output, the unnecessary gate drive signals are removed and the counter side switch can be controlled up to 100% PWM duty ratio with a smooth transition between different dead-time effect modes. That will maximize the dc-link voltage utilization and improve the harmonic distortion. Since the unnecessary gate drive signals are removed, the switching loss caused by the turn-off tail current can be reduced.

II. CIRCUIT AND CONTROL CONFIGURATION

A. Circuit Configurations

The inverter circuit is shown in Fig.1 and the parameters shown in Table 1 are used in the system. The inverter system consists of a dc/dc converter, a dc-link capacitor, a voltage source inverter, and an LC filter circuit. In this Figure, V_{dc} is the dc-link voltage, L_f and C_f are the inductor and capacitor of LC filter, and Z_L represents the load connected to the inverter output.

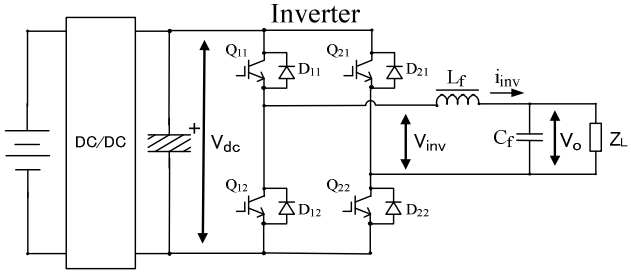

Fig. 1. Inverter Circuit Configuration.

TABLE I. SYSTEM PARAMETERS

Filter inductor	1mH
Filter capacitor	20uF
Carrier frequency	20kHz
Dead-time	3μs
Rated output power	1kVA

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B. *Conventional PID control*

Figure 2 shows the inverter control configuration and Fig. 3 shows the PID control block diagram. The PWM duty ratio is obtained by Eq. (1). To prevent the short circuit of dc-link voltage, dead-time is inserted between the commutations.

$$D = \frac{(u + V_o^*)/V_{dc} + 1}{2} \tag{1}$$

where u is the output of PID controller, V_o^* is the inverter voltage reference, and V_{dc} is the dc-link voltage.

Considering an ideal switch case, neglecting the non-ideal characteristics of the circuit components, the closed-loop transfer function of the inverter can be expressed as Eq. (2).

$$\frac{V_o}{V_o^*} = \frac{K_d s^2 + (1 + k_p)s + k_i}{L_f C_f s^3 + K_d s^2 + (1 + k_p)s + k_i} \tag{2}$$

where s is the Laplace operator, V_o^* is the reference of inverter voltage, K_p is proportional gain, K_i is the integral gain, and K_d is the derivative gain of the PID controller.

In the time domain, the derivative of inverter voltage can be expressed as Eq. (3).

$$\frac{de_v}{dt} = \frac{d\left(V_o^* - V_o\right)}{dt} = \frac{i_c^*}{C_f} - \frac{i_c}{C_f} \tag{3}$$

where i_c^* is the reference of capacitor current which can be obtained by Eq. (4), i_c is the capacitor current which can be measured directly, or calculated by the difference of inductor current and load current measurement result.

$$i_c^* = C_f \cdot \frac{dV_o^*}{dt} = \omega \cdot C_f \cdot \cos(\omega t) \tag{4}$$

In this paper, to alleviate the influence of measurement noise, the proportional control of capacitor current is adopted instead of the derivative calculation of output voltage.

With appropriate control parameters and a relative small dead-time, low distortion voltage output can be obtained at the inverter output. However, with a high switching frequency and when a relative large dead-time is applied, the dead-time effects give large influence on the inverter operations.

Figure 4 shows the output voltage simulation result at the condition of V_{dc}=180V. Due to the dead-time effect, on the positive side and the negative side near the zero crossing point, significant voltage distortions can be observed.

Figure 5 shows the simulation waveforms at the condition of V_{dc}=150V and the modulation signal is limited to less than 100% duty ratio. Together with the zero crossing distortion, the required voltage output can't be obtained.

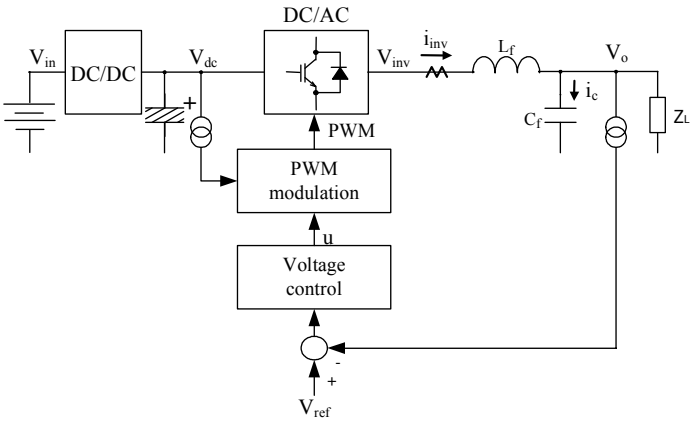

Fig. 2.Inverter control configuration.

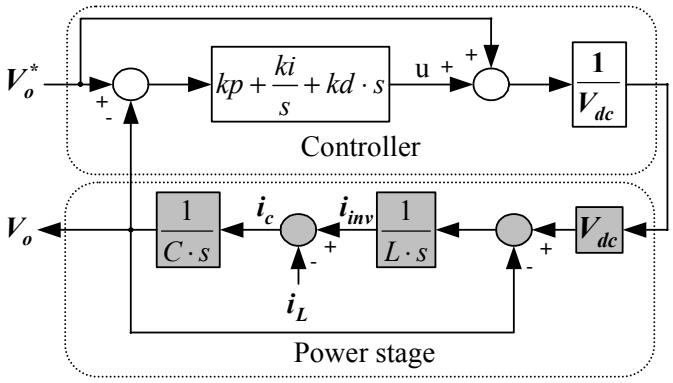

Fig. 3.Inverter voltage control block diagram (Conventional).

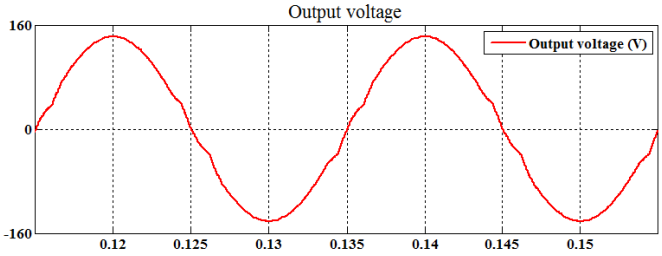

Fig. 4. Output voltage, Condition: V_{dc}=180V

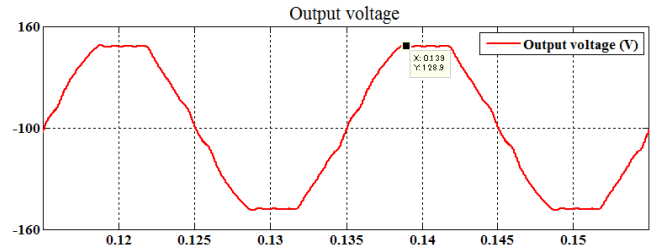

Fig. 5. Output voltage, Condition: V_{dc}=150V, modulation signal is limited to 0.4%-99.6% duty ratio.

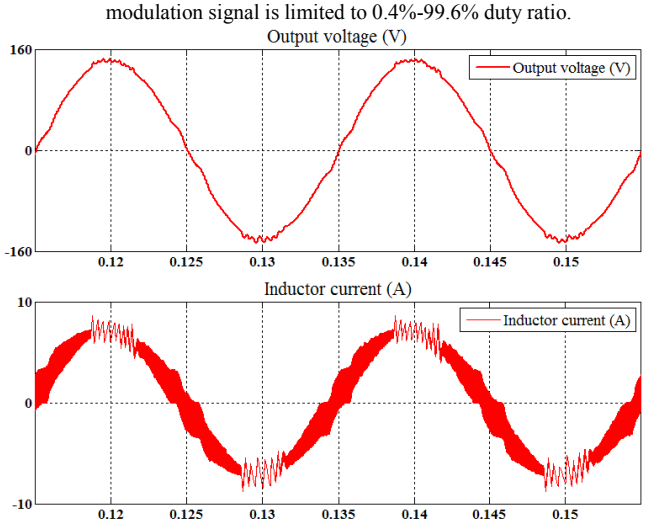

Fig. 6. Output voltage, Condition: V_{dc}=150V, without limitation of modulation index

As shown in Fig. 6, without the limitation of modulation signal, although the maximum voltage amplitude can be achieved, low frequency ripple voltage and ripple current occurs, that may results in large audible noise.

III. The Proposed Control Scheme

A. Dead-time effect

For grid-connected inverter, in reference [4], by analyzing the PWM modulation signals and the influence of switching ripple current, an accurate dead-time error mathematical model is developed. The model is shown in Fig. 7, in this model, the dead-time effects are divided into five modes according to the inductor current and the switching ripple current. In mode 1 and 5, a positive or a negative error voltage appears. In mode 2 and 4, instead of the inductance characteristics, resistive characteristics can be observed between the reference voltage (V_{ref}) and the inductor current. In mode 3, if the turn off delays of the positive switch and the negative switch are the same, ideal switch characteristics can be obtained.

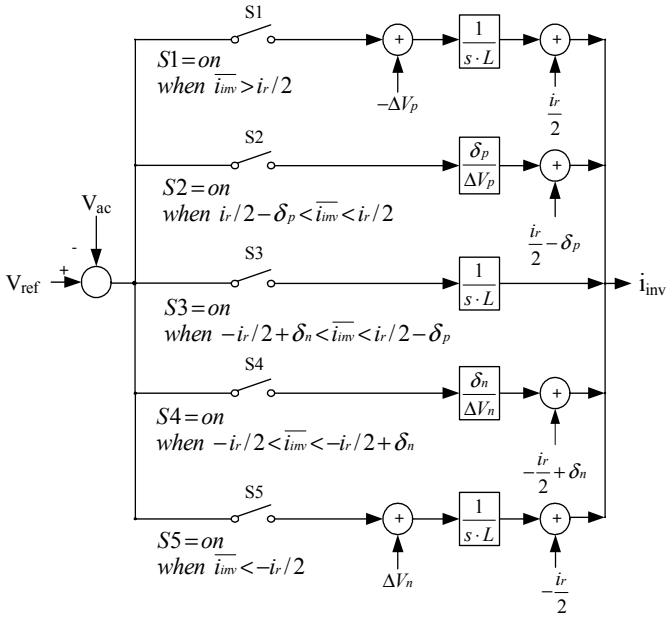

Fig. 7. Dead-time effect mathematical model.

This dead-time effect mathematical model can also be applied for CVCF inverters, including the non unity power factor load and the nonlinear load condition.

For the inverter circuit shown in Fig. 1, neglecting the turn on and turn off delay of the power switch. The dead-time error voltages of ΔV_p and ΔV_n can be expressed as Eq. (5).

$$\Delta V = \frac{2 \cdot T_d}{T_c} \cdot V_{dc} \tag{5}$$

Calculated by the parameters shown in Table I, the dead-time error voltage is 12% of the dc-link voltage; only 88% voltage transfer ratio can be obtained. To output the same voltage, the dc-link voltage should be 13.6% higher than the ideal switch condition.

B. The proposed Control Scheme

For the objective of attaining good performance under parameter and load variations, sliding mode control approaches were investigated for the power converter control [5-7]. In this paper, together with a linear PID controller, according to the dead-time model shown in Fig. 7, a sliding mode controller is proposed for the dead-time compensation of CVCF inverters.

Figure 8 shows the proposed controller configuration. The control scheme consists of a PID controller and a SMC controller. The PID controller operates in the linear operation areas; it is designed with the previous introduced method. The SMC controller detects the dead-time nonlinear operations and output the dead-time error voltage for the dead-time compensation. The details are presented hereafter.

Considering the nonlinear operations as model error of the linear model, the relation between the controller output and the inductor current can be expressed as Eq. (6).

$$V_{ref} = V_o + L_f \cdot \frac{di_{inv}}{dt} + \varepsilon \tag{6}$$

where V_{ref} is the modulation reference voltage, V_o is the output voltage, i_{inv} is the inductor current , L_f is the inductor inductance of LC filter, ε represents the model error caused by the nonlinear characteristics such as dead-time effect. With a PID controller and the feed forward of instant voltage reference, V_{ref} can be expressed as Eq. (7).

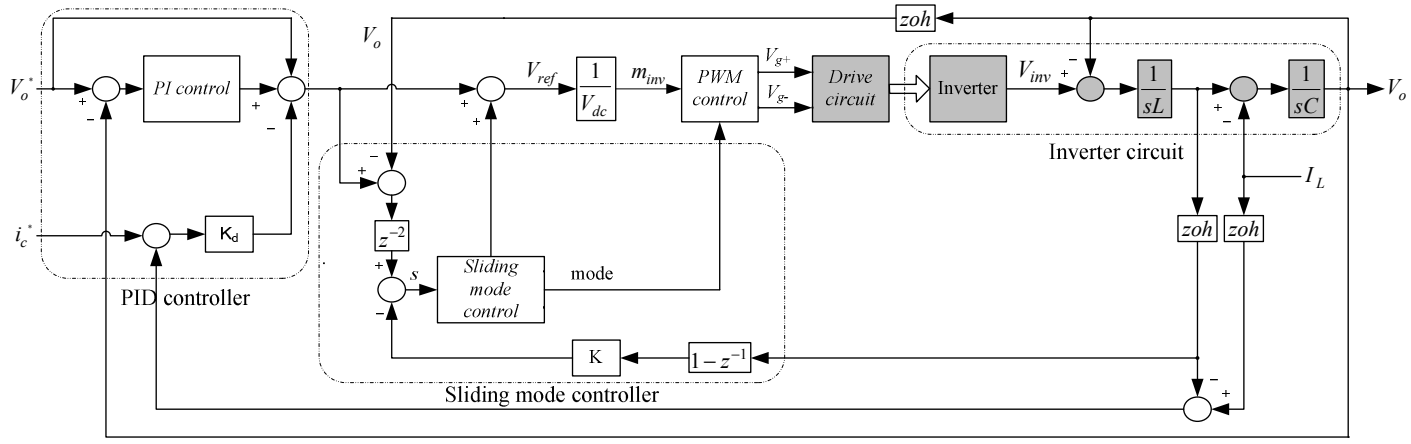

Fig. 8. The proposed voltage control scheme.

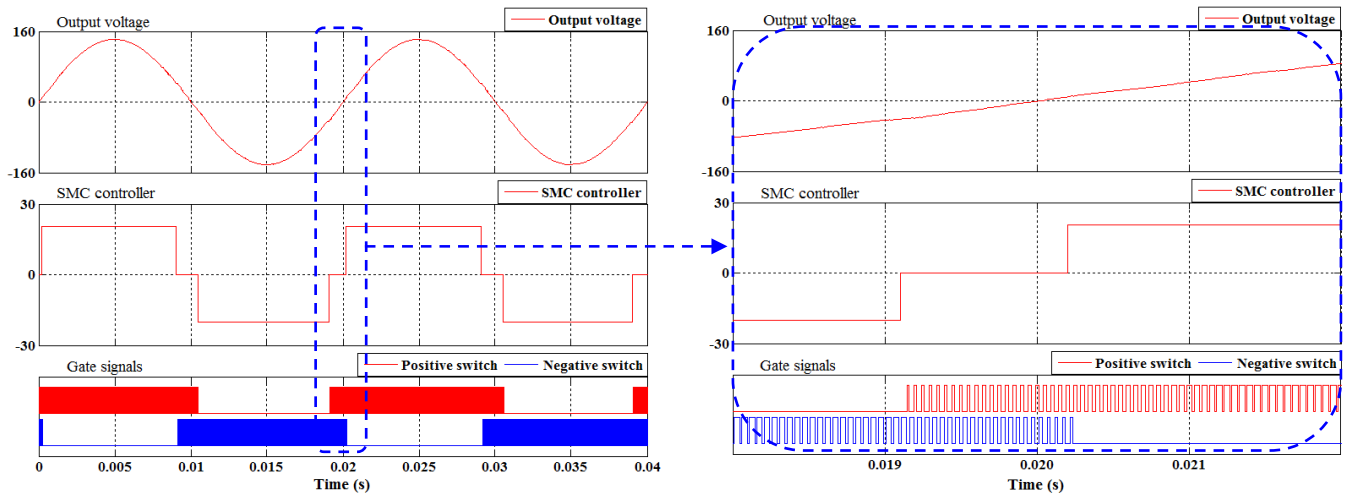

Fig. 9. PWM modulation gate control.

$$V_{ref} = K_p \cdot e + K_i \cdot \int e + K_d \cdot \dot{e} + V_o^* \quad (7)$$

The derivative of inductor current can be approximated as Eq. (8).

$$di_{inv}/dt = \left(i_{inv}(n) - i_{inv}(n-1)\right)/T_c \quad (8)$$

where T_c is the switching period. Because the dead-time error voltage is the major part of the model error. From Eqs. (6), (7) and (8), a sliding mode function shown in Eq. (9) can be obtained.

$$S = K_p \cdot e + K_i \cdot \int e + K_d \cdot \dot{e} + V_o^* - V_o - K \cdot \left(i_{inv}(n) - i_{inv}(n-1)\right) \quad (9)$$

With this function, the SMC controller outputs the dead-time compensation signal according to the control law defined in Eq. (10).

$$u_n = \begin{cases} \Delta V_p & \text{when } (S > \varepsilon) \text{ and } (u_{n-1} \geq 0) \\ 0 & \text{when } ((S > \varepsilon) \text{ and } (u_{n-1} < 0)) \text{ or} \\ & \quad ((S < -\varepsilon) \text{ and } (u_{n-1} > 0)) \\ -\Delta V_n & \text{when } (S < -\varepsilon) \text{ and } (u_{n-1} \leq 0) \\ \text{unchanged otherwise} \end{cases} \quad (10)$$

where ΔV_p and ΔV_n represents the positive and the negative dead-time error voltage that can be calculated by the dead-time value and adjusted by a parameter auto-tuning method. The hysteresis of ε is applied to avoid the control chattering and eliminate the influence by measurement noise.

C. Switch Gate Drive Control

Figure 9 shows the PWM modulation gate control operation. The gate signals of Q_{11} and Q_{12} are shown in this figure. When the SMC controller outputs a positive value, the gate signal of negative switch Q_{12} is removed and the positive switch Q_{11} is controlled by a PWM signal without inserting the dead-time. If the SMC controller outputs a negative value, the positive switch gate signal is removed. Otherwise, both of the switch gate signals are controlled on/off with a dead-time inserted between the commutations. Because the unnecessary charge and discharge of the IGBT internal gate is eliminated, the tail current loss can be reduced.

IV. Simulation Verification

The proposed voltage control and PWM modulation control scheme are verified in MATLAB/Simulink and SimPower-Systems simulation environment. The control algorithm is implemented by MATLAB language code.

The inverter circuit shown in Fig. 1 and the parameters shown in Table I are used for the simulation. The comparisons between the PID controller without the dead-time compensation and the proposed controller are presented in this section.

Figure 10 shows the waveforms of the proposed control

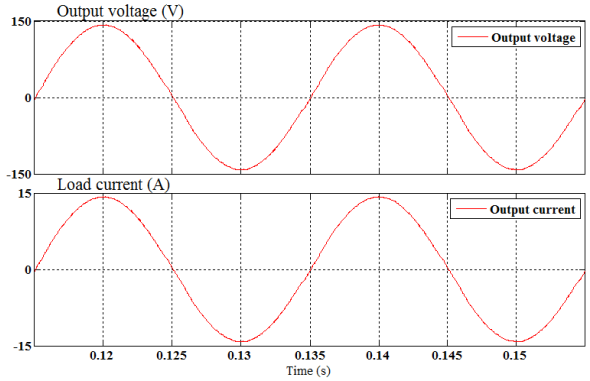

Fig. 10. Simulation waveforms with rated resistive load. V_{dc}=180V.

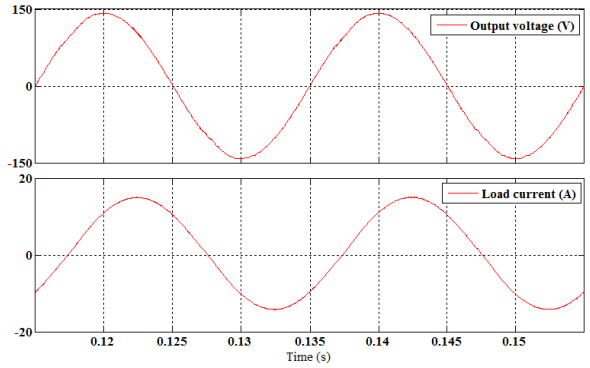

Fig. 11. Simulation waveforms with rated 0.7 lagging power factor load, V_{dc}=180V.

with a rated resistive load. Compared with the waveform shown in Fig. 4, the harmonic distortion is greatly reduced.

Figure 11 shows the waveforms of the proposed control with a 0.7 lagging power factor load, low distortion output is obtained in the none unity power factor load condition.

Figure 12 shows the waveforms with a rectifier load. The crest factor is about 2.97, with a peak current of 18.6A. The effectiveness is confirmed in the nonlinear load condition.

Figure 13 shows the waveforms with a decreased dc-link voltage, compared with the voltage waveform shown in Fig. 5, a low distortion and the desired voltage can be obtained. With the proposed control method, the dc-link voltage can be decreased from 170V to 150V. 20V reduction of dc-link voltage can be achieved.

Figure 14 shows the voltage THD (total harmonic distortion) comparison with resistive load. In all of the load range, the total harmonic distortion decreases to about 1/3-1/2 of the conventional.

Figure 15 shows the voltage THD (total harmonic distortion) comparison with rectifier load. The total harmonic distortion decreases to about 1/3-2/3 of the conventional.

Figure 16 shows the transient response of the inverter with the load changing from no load to the rated resistive load. The inverter provides fast response to the load change transient.

Figure 17 shows the inductor ripple current decrease. The decreases of dc-link voltage from 170V to 150V will contribute to a 19% reduction of inductor switching ripple current. The iron losses can be reduced by a corresponding level.

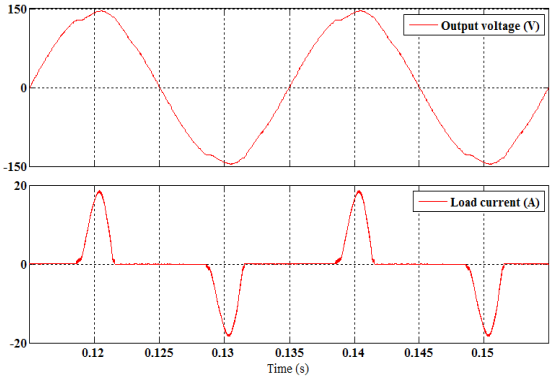

Fig. 12. Simulation waveforms with rectifier load, V_{dc}=180V

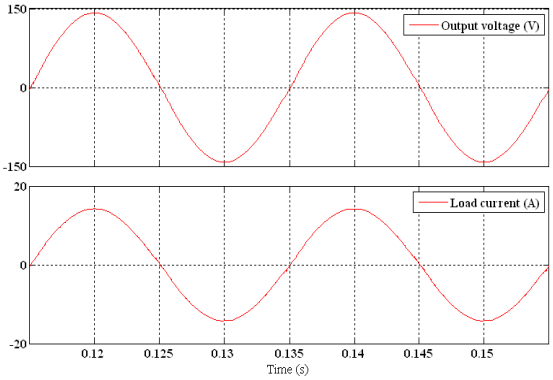

Fig. 13. Simulation waveforms with resistive load, V_{dc}=145V.

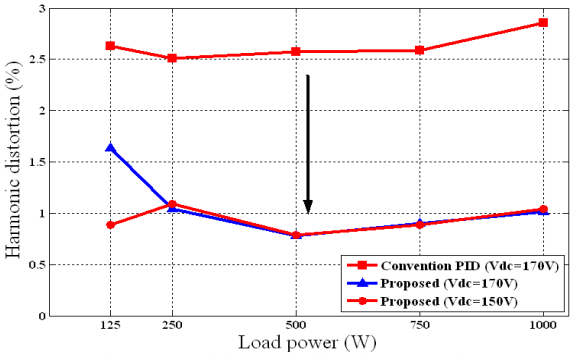

Fig. 14. Total harmonic distortion comparison with resistive load.

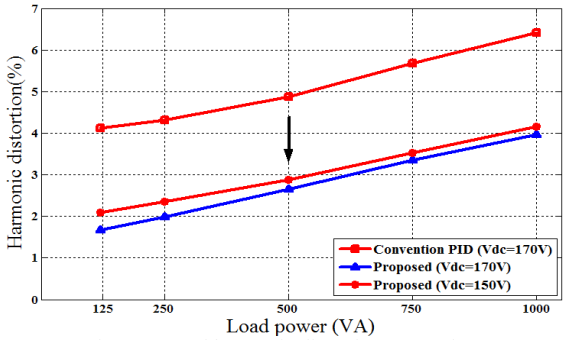

Fig. 15. Total harmonic distortion comparison with rectifier load.

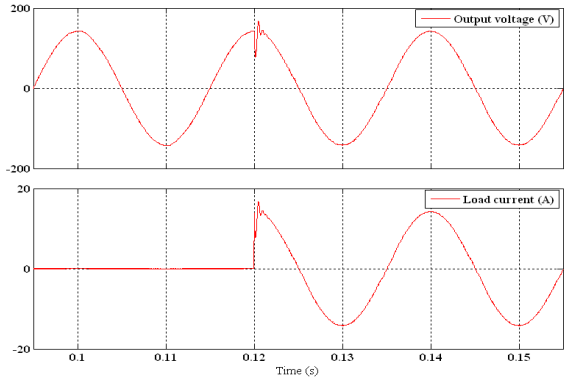

Fig. 16. Load change from no load to the rated load.

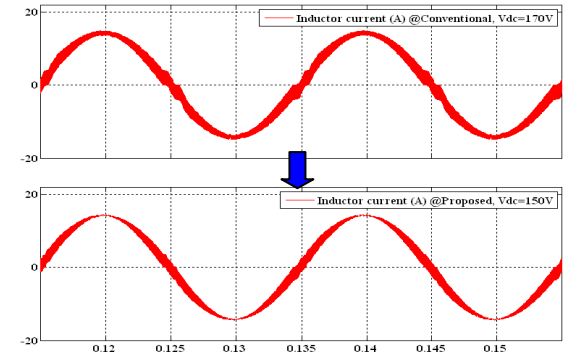

Fig. 17. Inductor current of AC filter. (Switching ripple component: 0.858Arms->0.696Arms).

V. CONCLUSION

This paper presented a new voltage control and PWM modulation gate control scheme for dead-time compensation of CVCF inverters. The proposed control scheme consists of a SMC controller and a PID voltage controller. The SMC controller detects the dead-time nonlinear operations and operates for the dead-time compensation; the PID controller operates in the linear areas. In this control scheme, the PWM modulation gate drive is divided into three operation modes according to the SMC controller output. The unnecessary gate drive signals are removed and the counter side switches are controlled up to truly 100% PWM duty ratio with a smooth transition between different modulation modes. With this control scheme, the influence of dead-time can be eliminated, and the harmonic distortion can be greatly reduced. The minimization of dc-link voltage will contribute to a reduced switching loss and a small inductor ripple current. Compared with the conventional PID control, the following improvements are confirmed by simulation results.

(1) The harmonic distortion is decreased to about 1/3-1/2 of the conventional, the effectiveness are also confirmed in the non unity power factor load and nonlinear load condition.

(2) In the studied system, the dc-link voltage can be reduced by about 14%. The inductor ripple current is reduced by about 19%. With a lower dc-link voltage, the dc-link capacitor size can be reduced.

(3) With a low dc-link voltage, and the new gate drive control strategy, the efficiency improvements can be expected.

The proposed control scheme will be experimented in a DSP controller based inverter system, and only some program codes are needed.

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