A Novel Implementation of an FPGA-Based Controller for Conducted-Noise Reduction in Randomly Switched DC-DC Converters

Gamal M. Dousoky[1)] Masahito Shoyama[1)] Tamotsu Ninomiya[2)]

1) Kyushu University, 744 2-626-1 motooka, nishi-ku, Fukuoka, 819-0395 Japan
2) Nagasaki University, 1-14 Bunkyo-machi, Nagasaki, 852-8521 Japan

E-mail: dousoky@ieee.org

***Abstract*- This paper proposes a novel implementation of an FPGA-Based controller for conducted-noise reduction in dc-dc converters. The switching noise produced by the converter has been reduced by randomly varying the switching frequency of the converter. Traditionally, the implementation of the switching-mode power supply (SMPS) has been accomplished using analog control circuits. However, the field-programmable gate array (FPGA) is much flexible than analog control circuits, becoming lower cost, and applicable for power supply applications. The implementation of the SMPS has been accomplished using FPGA-based digital controller. Moreover, breadboard has been built-up for testing the effect of using the proposed FPGA-based digital controller for noise reduction in dc-dc converters. Experimental results show that the conducted-noise spectrum has been significantly improved and the noise level has been effectively reduced.**

***Keywords*: Noise Reduction, Random Switching, SMPS, DC-DC Converter, EMI, EMC, FPGA.**

I. INTRODUCTION

Power electronics has become the dominant factor in the deterioration of our electromagnetic environment, causing declining quality of line power and increasing level of conducted electromagnetic interference (EMI), [1].

In general, more significant is the contribution of periodically operated semiconductor switches (rectifiers, SCRs and triacs, BJTs, MOSFETs, and IGBTs). The semiconductor switches produce differential-mode conducted EMI through the basic power-conversion process and common-mode conducted EMI through capacitive or inductive coupling, [1]-[2].

The recent electromagnetic compatibility (EMC) regulations recognize the need for reducing the harmonic pollution of the power line, and limit the amount of harmonic current emission.

Traditional solutions are related to filters and shielding techniques. However these solutions have a number of limitations and drawbacks, which exclude universal applicability. Alternative, random-switching technique attenuates the switching noise by spreading them over frequency range. This is typically achieved by randomly varying the switching frequency of the switching power supplies. Random-switching control is effective for suppressing the peak level of switching-noise spectrum, [2]-[3].

Hardware limitations and the complexity of the control circuits cause difficulty in achieving compliance with standard EMC regulations while maintaining low conducted EMI and low cost. On the other hand, with the flexibility and programmability of the FPGA technology, many attractive techniques can be designed and implemented as well, [4]. The implementation of the proposed controller has been accomplished using FPGA technology.

The paper is organized as follows: Section II describes the converter power-circuit design, analog to digital conversion circuit and its driver, and the proposed FPGA-based digital controller which includes digital compensator, pseudorandom stream generator, and digital pulse-width modulator. Section III presents details of the experimental test circuit. Experimental results and analysis are presented in Section IV. Finally, conclusions have been presented in section V.

II. RANDOMLY SWITCHED DC-DC CONVERTER USING FPGA

Fig. 1 illustrates the over-all circuit block diagram of randomly switched dc-dc converter using an FPGA. It consists of dc-dc power switching circuit, analog to digital conversion circuit and its driver, the proposed FPGA-based digital controller, and interface and power switches driver.

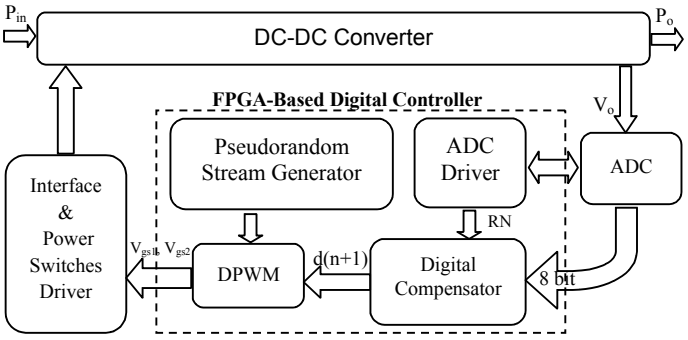

Fig.1. Block diagram of randomly switched dc-dc converter using FPGA-based digital controller.

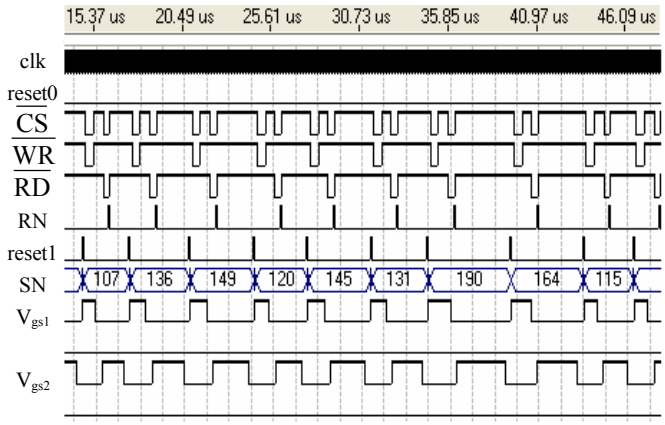

Fig. 2. VHDL simulation of the proposed FPGA-based digital controller.

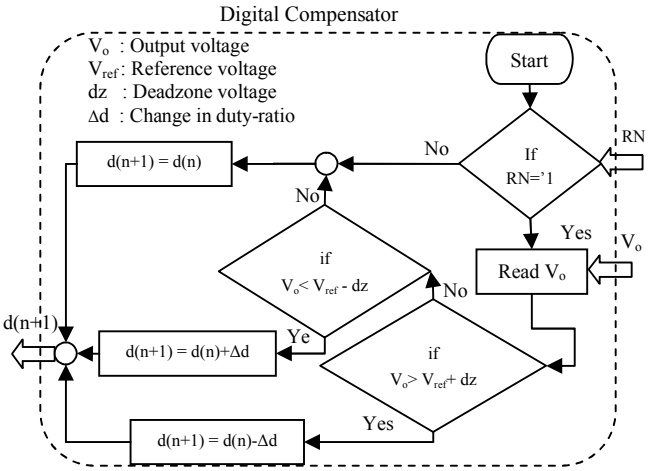

Fig. 3. Flowchart of the designed digital compensator.

A. Converter Power-Circuit Design

A synchronous buck converter topology has been selected in order to improve efficiency and reduce heat loss, [5]. The output inductor and capacitor have been sized such that:

- The converter operates in continuous conduction mode (CCM) at minimum output current.
- The peak-to peak value of ripple voltage within Vr = 20 mV.
- Current ripple ratio r ≈ 0.4.

B. Analog to Digital Conversion Circuit and Its Driver

The converter output voltage is converted into a digital 8-bit signal by means of analog to digital converter (ADC). This signal is processed by the digital compensator to calculate the duty-ratio (d). The ADC's driver is designed and imbedded in the FPGA-based digital controller. As shown in Fig. 2, $\overline{RD}$ is brought low after the rising edge of $\overline{WR}$. This completes the conversion and enables the output buffers that contain the conversion result. Read-now (RN) signal is brought high after the falling edge of $\overline{RD}$, which commands the digital compensator to read the conversion result. The conversion cycle is started with the switching cycle and completed within the same switching cycle.

C. Digital Compensator

In order to regulate the output voltage to match a precise voltage reference over a range of input voltage values, load currents, and temperature variations, a digital compensator has been designed. Moreover, the digital compensator makes the output voltage immune to the randomized variation in the switching frequency. As illustrated in Fig. 3, during the current switching cycle, the digital compensator computes a digital duty-ratio (d(n+1) for the next switching cycle). It can be seen that when the output voltage approaches the desired value, the duty cycle is frozen. In this way, a stable operating condition is obtained. Thus, the use of deadzone comparator prevents undesired oscillations at the converter output.

D. Pseudorandom Stream Generator

A pseudorandom stream generator has been constructed as shown in Fig. 4. The proposed construction uses several maximum length linear feedback shift registers (m-LFSRs) in parallel. The using of m-LFSRs is due to the fact that the sequence generated by the m-LFSRs has a maximum period. For different m-LFSRs output bits, different initial contents of m-LFSRs (seeds) have been used.

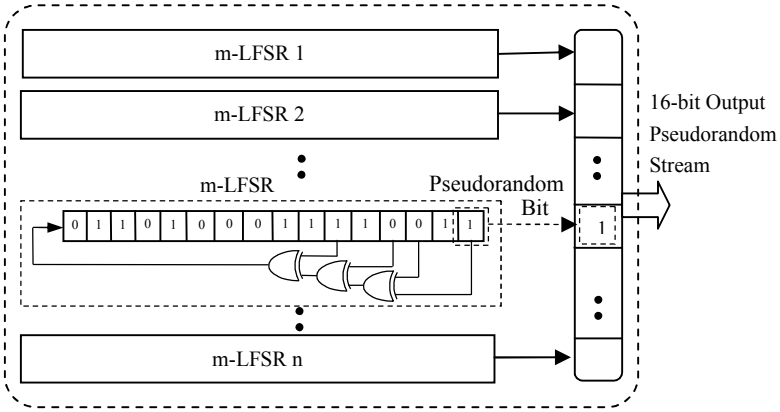

Fig. 4. The proposed pseudorandom stream generator.

The taps are XOR'd sequentially with the output and then fed back into the leftmost bit. The designed pseudorandom stream generator delivers a 16-bit output; (maximal number is 2^{16} -1= 65535).

The random stream is composed of the output bits of the component m-LFSRs. The component m-LFSRs are clocked regularly; i.e., the movement of the data in all the m-LFSRs is controlled by the same clock. Only at the beginning of every switching cycle, the random output bits are converted into an integer number (PRN) and used in the digital pulse-width modulator (DPWM). However, the other generated random output bits are discarded.

E. Digital Pulse-Width Modulator

At the beginning of every switching cycle, the DPWM achieves the following assignments:

1. Taking d(n+1) as input, considering it as the duty-ratio of the started switching cycle (d(n)).
2. Converting the pseudorandom output bits into an integer number (PRN).
3. Calculating switching frequency for the started switching cycle and the needed number of clocks (SN) to fulfill it as follows:

$$f_{sw} = f_L + K * PRN \quad (1)$$
$$SN = f_{clk} / f_{sw} \quad (2)$$
$$DN = SN * d(n) \quad (3)$$

Where;

- f_{sw} : Switching frequency
- fL : Lower frequency limit
- K : Constant for achieving the required randomized frequency range
- PRN : Pseudorandom output stream converted into integer number
- SN : Needed number of steps to fulfill the switching frequency
- f_{clk} : Clock frequency
- DN : Needed number of steps to fulfill the duty-ratio

As shown in Fig. 2, the designed DPWM uses a clocked-counter that increments (up to SN) and resets at the end of the switching cycle of the PWM (see reset1 signal). When the counter value exceeds the reference value (DN), the PWM output changes state from high to low. In this way, the digital pulse-width modulated waveforms ($V_{gs1,2}$) with the commanded duty-ratio at the calculated switching frequency are generated.

III. Experimental Work

The randomly switched dc-dc converter, described in section II, has been designed and implemented using an Altera FPGA. Table I illustrates the synchronous buck converter parameters. The measured efficiency of the converter at different switching frequencies is shown in Fig. 5. Moreover, the effect of using the proposed controller on the converter output characteristics is illustrated in Fig. 6. It is clear that the output voltage has been well regulated using the proposed controller.

The conducted-noise has been measured across the input terminals of the converter using line impedance stabilization networks (LISN), [3]. Fig. 7 describes experimental circuit for conducted noise measurements. The LISN is used to standardize the input impedance seen from the converter input and sense the conducted-noise, which is measured by an EMI receiver.

TABLE I
THE SYNCHRONOUS BUCK CONVERTER PARAMETERS.

Symbol	Description	Value
V_{in}	Input voltage (V)	12
V_o	Output voltage (V)	3.3
I_o	Output current (A)	5
f_{csw}	Center switching frequency (kHz)	300
L	Output inductor (µH)	4.3
C	Output capacitor (µF)	470
C_{in}	Input capacitor (µF)	100

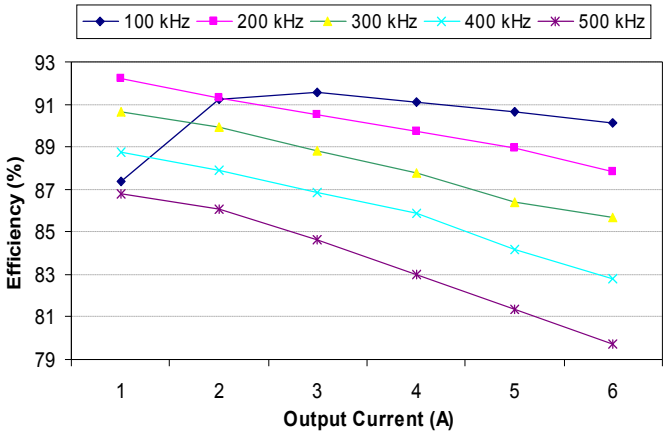

Fig. 5. Measured efficiency of the designed converter (at V_{in} = 12 V and d = 0.3).

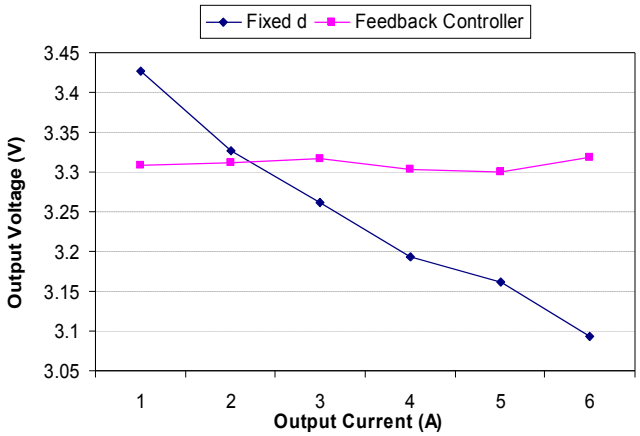

Fig. 6. The effect of using the proposed controller on the converter output characteristics (at Fsw = 300 kHz, Vin = 12 V and d = 0.3).

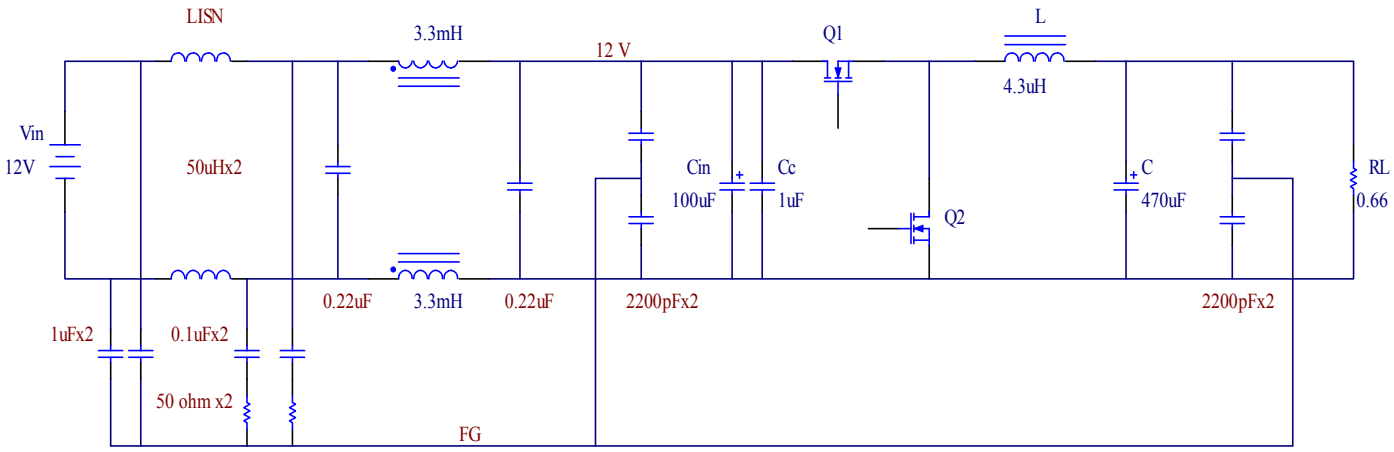

Fig. 7. Experimental circuit for conducted-noise measurements.

In order to investigate the effect of random-switching on the conducted-noise characteristics of the buck converter using FPGA, three factors have been studied as follows:

1. FPGA clock speed, (20 MHz, 40 MHz, and 66 MHz speeds have been used).
2. Randomization ratio percentage, (RRP):

$$RRP = \frac{K*PRN}{2*f_{csw}}*100 \quad (4)$$

Where;

RRP Randomization ratio percentage,

f_{csw} Center switching frequency.

3. Using the feedback controller (FB) / fixed duty-ratio (Fixed d).

IV. Results and Analysis

As illustrated in Fig. 8, the noise level reduction increases with using higher FPGA clock speed, since the randomization resolution increases.

In other words, any output signal of the FPGA is composed of number of clocks. Then, the frequency of this output signal can be calculated by the following equation:

$$F_{output\ signal} = \frac{1}{\text{clocks No.}*T_{clk}} = \frac{f_{clk}}{\text{clocks No.}} \quad (5)$$

Where;

$F_{output\ signal}$ Frequency of the output signal

T_{clk} Time period of each clock cycle = $1/f_{clk}$

From the above equation, for an output signal with a certain frequency randomization range, higher FPGA clock speed permits wider range of clocks number (i.e. larger number of different frequencies), that means higher randomization resolution as illustrated in Fig. 9. On the other hand, the higher FPGA clock speed, the higher FPGA cost.

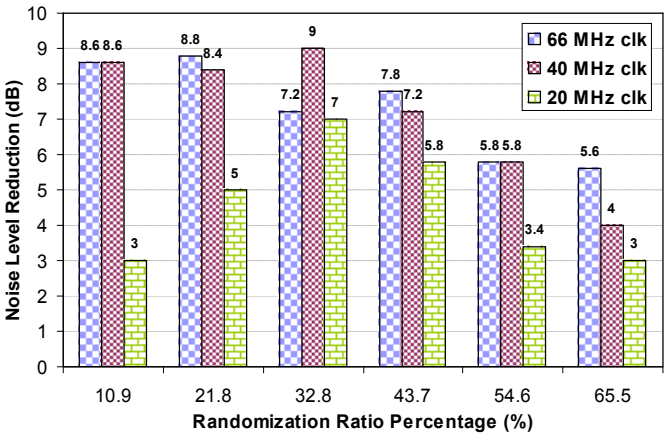

Fig. 8. The effect of FPGA clock speed on the noise level reduction.

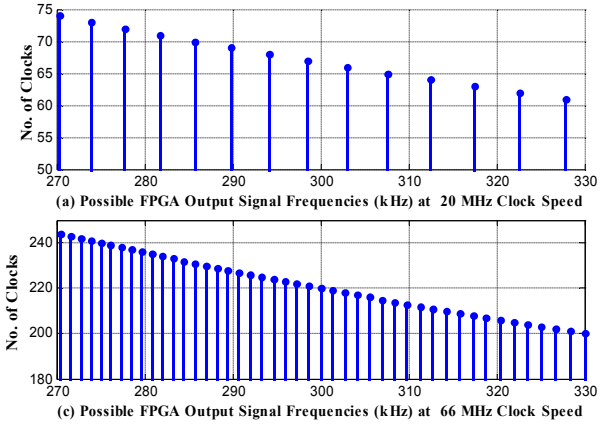

Fig. 9. The effect of increasing the FPGA clock speed on the randomization resolution (for 270~330 kHz output signal).

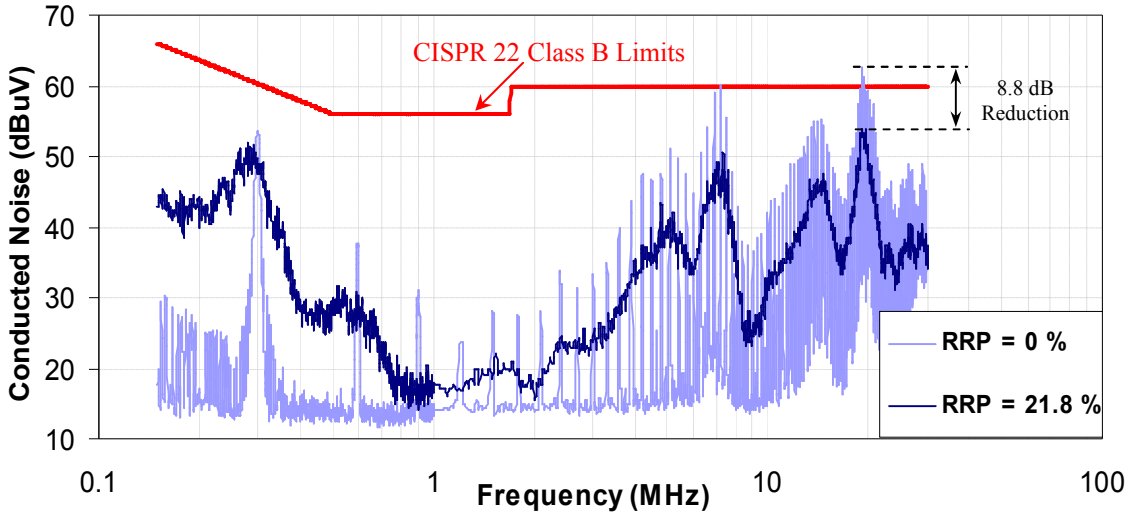

Fig. 10. Comparison between the spectrum of the conducted-noise of the buck converter with fixed switching frequency (0% RRP) and that with randomized switching frequency (21.8% RRP), (at f_{clk} = 66 MHz and using the FPGA feedback controller).

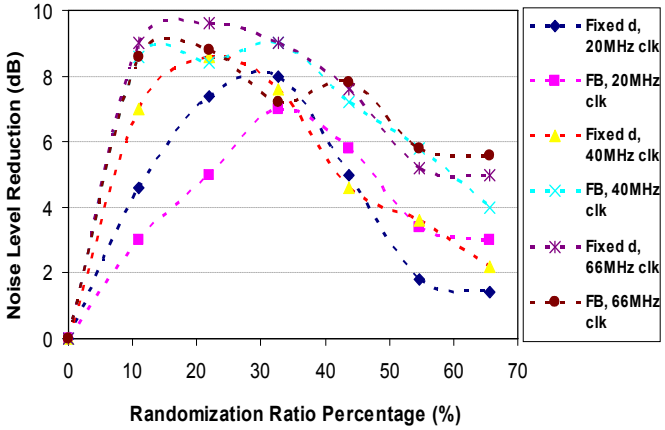

Fig. 11. The effect of randomization ratio percentage on the noise level reduction.

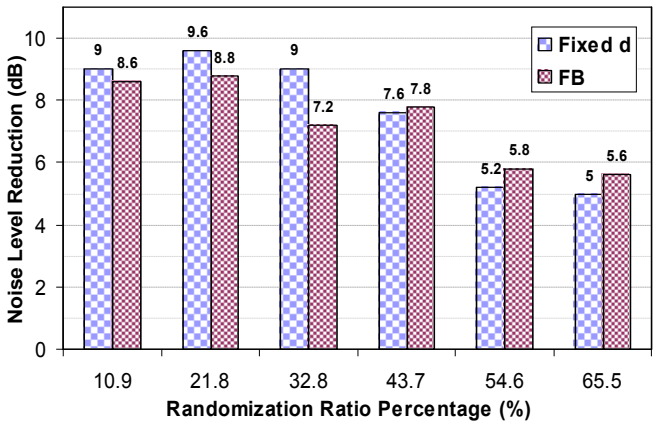

Fig. 12. The effect of using the feedback controller on the noise level reduction (at f_{clk} = 66 MHz).

The comparison, shown in Fig. 10, reveals that the conducted-noise spectrum has been significantly improved and the noise level has been effectively reduced.

As presented in Fig. 11, increasing the randomization ratio increases the noise level reduction until a certain ratio where the noise level reduction again decreases. The latter is due to the overlaps between the successive frequency spectrum ranges. Fig. 12 shows the effect of using the feedback controller on the noise level reduction. It is clear that, the feed back controller regulates the output voltage effectively. However, it slightly decreases the noise level reduction.

V. Conclusions

A novel FPGA-based controller has been designed and implemented for conducted-noise reduction in dc-dc converters. Moreover, the effect of using the proposed controller on the conducted-noise characteristics of the converter has been experimentally investigated. It can be concluded that:

Increasing the FPGA clock speed improves the conducted-noise spectrum of the converter. The feed back controller regulates the output voltage effectively. However, it slightly attenuates the noise reduction. Furthermore, increasing the randomization ratio increases the noise reduction until a certain ratio where the noise reduction again decreases.

Finally, experimental results show that, using the proposed FPGA-based controller, the conducted-noise spectrum has been significantly improved and the noise level has been effectively reduced.

References

[1] R. Redl, "Power Electronics and Electromagnetic Compatibility", IEEE PESC'1996, vol. 1, pp.15-21, Jun 1996.

[2] T. Tanaka, T. Ninomiya, and K. Harada, "Random-Switching Control in DC-to-DC Converters", IEEE PESC'1989, vol. 1, pp. 500-507, Jun 1989.

[3] C.R. Paul, "Introduction to Electromagnetic Compatibility", John Wiley & Sons, New York, 2nd edition, 2006.

[4] "What Is the Next Implementation Fabric?", IEEE Design and Test of Computers ,vol. 20, no. 6, pp. 86-95, Nov/Dec, 2003.

[5] R. Miftakhutdinov, and J. Zbib, "Synchronous Buck Converter with Increased Efficiency", IEEE APEC '2007, pp. 714-718, Mar 2007.