FPGA-Based Design and Implementation of Spread-Spectrum Schemes for Conducted-Noise Reduction in DC-DC Converters

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***Abstract*- In this paper many spread-spectrum schemes, several of which are new, have been designed and implemented for conducted-noise reduction in DC-DC converters. A field-programmable gate array (FPGA) has made substantial improvements in price and performance throughout the past few years. The implementation of the schemes has been accomplished by using FPGA-based controller.**

A breadboard circuit has been built-up for investigating the effect of all the proposed schemes on conducted-noise spectrum in DC-DC converters. Furthermore, a comparative study has been carried-out to reach the most efficient scheme in spreading the conducted-noise spectrum.

Experimental results show that randomizing each of carrier frequency, duty-ratio, and the pulse position parameters significantly improves the conducted-noise spectrum and effectively reduces the noise peaks at both high and low frequency ranges.

I. INTRODUCTION

DC-DC converters are important in portable electronic devices such as cellular phones , laptop computers, and electric vehicles, which are supplied with power from a DC power source such as batteries, photovoltaic cells, or fuel cells. Such electronic devices often contain several sub-circuits, with each sub-circuit requiring a unique voltage level different from that supplied by the source, [1] - [3].

Switching power converters have been reported to generate common-mode and differential-mode conducted-noise in addition to radiated-noise. They may cause serious problems by generating such switching noise. Although switching converters produce significant amounts of switching noise, they are also required to operate inside electromagnetic interference (EMI) sensitive applications, [4] and [5]. This research aims to reduce the switching noise produced by DC-DC converters.

Traditional tools for EMI suppression are related to the use of filters and shielding techniques. But these tools are bulky and require expensive passive components, which makes them unsuitable for space-limited and price-sensitive portable devices, [5] and [6].

Alternative, pre-emptive EMI mitigation techniques eliminate the need for EMI filters by spreading the switching converters noise over a frequency range, [7]–[14]. By using these techniques, the noise generated by the Switching-Mode Power Supplies (SMPS) can be spread across a well defined frequency band. As a result, the average spectral power density of the broadband noise can thus be drastically reduced, [15].

FPGA is an attractive hardware design option. It has made substantial improvements in price and performance throughout the past few years, [16]. For an excellent overview of the classical and recent developments in FPGA technology, focusing on industrial control system applications, the reader is referred to [17]. Although FPGA implementation is now widespread in a range of military, defense, and signal processing applications, it is much flexible than analog control, becoming lower cost, and applicable for power supply applications. The implementation of the spread-spectrum schemes has been accomplished by using FPGA-based digital controller.

The paper is organized as follows: Section II presents spread-spectrum schemes in DC-DC converters. The design and implementation of the proposed FPGA-based controller which includes pseudorandom streams generator and digital pulse-width modulator are addressed in section III. Section IV describes the details of the experimental test circuit. Experimental results and discussion are presented in section V. Finally, conclusions and future work have been presented in section VI.

II. SPREAD-SPECTRUM SCHEMES IN DC-DC CONVERTERS

According to Fig. 1, T_k is the duration of the k^{th} cycle, α_k is the duration of the on-state within this cycle, and ε_k is the delay from the starting of the switching cycle to the turn-on within the cycle. Note that the duty ratio is $d_k= \alpha_k/ T_k$ and the switching frequency $F_k=1/T_k$.

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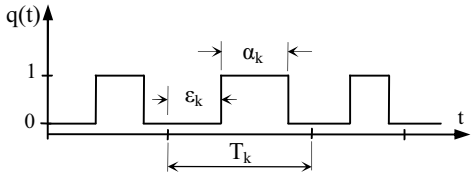


Fig. 1. Randomization parameters in the switching signal.

The switching function q(t) consists of a series of such switching cycles. In order to spread the frequency spectrum of the switching noise, {F_k, d_k, or ε_k} can be randomized. Table I summarizes all the possible schemes that can be carried-out for this purpose.

Some randomization schemes used in power electronics are, [7] - [14]:

- Randomized pulse position modulation (RPPM): ε_k changes; F_k, and d_k are fixed;
- Randomized pulse width modulation (RPWM): d_k changes; F_k, and ε_k are fixed;
- Randomized carrier frequency modulation with fixed duty ratio (RCFMFD): F_k, changes; d_k, and ε_k are fixed;
- Randomized carrier frequency modulation with variable duty ratio (RCFMVD): F_k, and d_k change; ε_k is fixed.

On the other hand, as in Table I, still another three different randomization schemes which haven't been addressed before; due to hardware limitations and the complexity of the control circuit. These schemes are:

- Randomized duty ratio, randomized pulse position modulation with fixed carrier frequency (RDRPPMFCF): d_k, and ε_k change; F_k is fixed;
- Randomized carrier frequency, randomized pulse position modulation with fixed duty ratio (RCFRPPMFD): F_k, and ε_k change; d_k is fixed;
- Randomized carrier frequency, randomized duty ratio, with randomized pulse position modulation (RRRM): F_k, d_k, and ε_k change.

TABLE I
THE RANDOMIZATION PARAMETERS FOR THE SCHEMES.

Case	Scheme	Randomization Parameters			α_k	Remarks
		F_k	d_k	ε_k		
(a)	PWM	Const.	Const.	Const.	Const.	Basic
(b)	RPPM	Const.	Const.	Rand.	Const.	Ad.*
(c)	RPWM	Const.	Rand.	Const.	Rand.	Ad.*
(d)	RDRPPMFCF	Const.	Rand.	Rand.	Rand.	New
(e)	RCFMFD	Rand.	Const.	Const.	Rand.; Synch.	Ad.*
(f)	RCFRPPMFD	Rand.	Const.	Rand.	Rand.; Synch.	New
(g)	RCFMVD	Rand.	Rand.	Const.	Rand.	Ad.*
(h)	RRRM	Rand.	Rand.	Rand.	Rand.	New

Ad.*: Addressed before in power electronics publications.

Now, with the flexibility and programmability of the FPGA technology, the above new schemes have been designed, implemented and addressed in this paper. Moreover, the other schemes, used before in power electronics, have been designed and implemented as well. Furthermore, all schemes have been experimentally investigated and conducted-noise spectrums have been compared in the following sections.

III. DESIGN AND IMPLEMENTATION OF THE PROPOSED FPGA-BASED CONTROLLER

This section presents the design and implementation of the proposed FPGA-based controller which includes pseudo-random stream generator and digital pulse-width modulator.

A. Pseudorandom Streams Generator

As discussed in the previous section, in order to spread the noise spectrum, {F_k, d_k, or ε_k} can be randomized. Hence three random number generators are needed to realize all the addressed schemes.

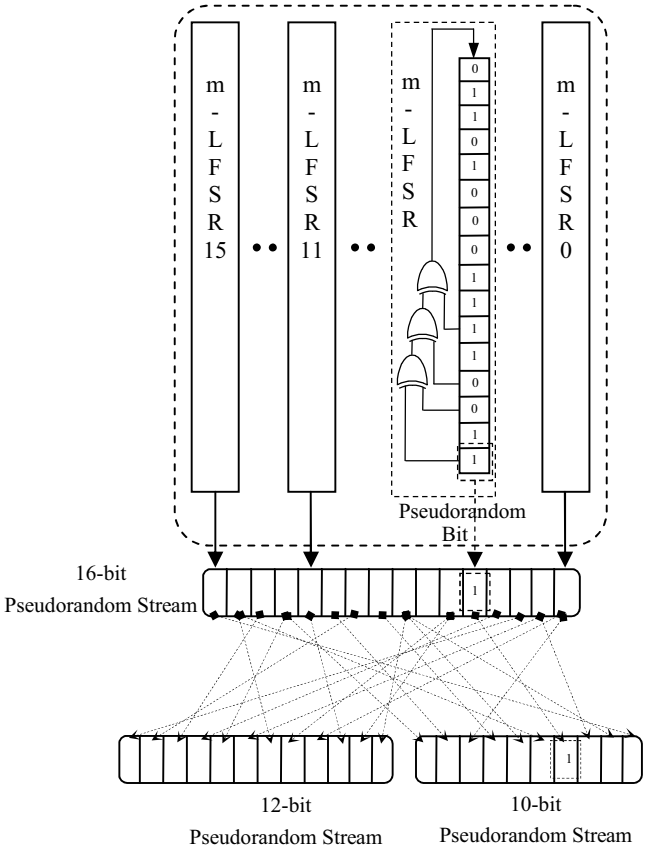


Fig. 2. The proposed pseudorandom streams generator.

A pseudorandom streams generator has been constructed for this purpose. As shown in Fig. 2, the proposed construction uses several maximum length linear feedback shift registers (m-LFSRs) in parallel. The use of m-LFSRs is due to the fact that the sequence generated by the m-LFSRs has a maximum period. For different m-LFSRs output bits, different initial contents of m-LFSRs (seeds) have been used. The taps are XOR'd sequentially with the output and then fed back into the leftmost bit.

The designed pseudorandom streams generator delivers three different random streams; (16-bit, 12-bit, and 10-bit streams). The 16-bit stream is composed of the output bits of the m-LFSRs. Furthermore, the 12-bit and 10-bit streams are composed of some of these bits with different arrangements. The m-LFSRs are clocked regularly; i.e., the movement of the data in all the m-LFSRs is controlled by the same clock.

Only at the beginning of every switching cycle, the random output bits are converted into an integer numbers (RFS, RDS, and RES) and used in the digital pulse-width modulator (DPWM). However, the other generated random output bits are discarded.

B. Digital Pulse-Width Modulator

At the beginning of every switching cycle, the DPWM achieves the following assignments:

1. Converting the pseudorandom (16-bit, 10-bit and 12-bit) streams into integer numbers (RFS, RDS and RES) with ranges from zero to (65535, 1023 and 4095), respectively.
2. Calculating randomization parameters for the started switching cycle and the needed number of steps to fulfill them as in the following equations:

$$f_{sw} = f_L + K * RFS \quad (1)$$

$$TN = f_{clk} / f_{sw} \quad (2)$$

$$WN = TN * (d_L + RDS)/1E4 \quad (3)$$

$$EN = TN * (e_L + RES)/ 1E4 \quad (4)$$

Where;

f_{sw}	: Switching frequency
f_L	: Lower frequency limit, (taken 234.5 kHz)*
K	: Constant (taken K=2*) for achieving the required randomized frequency range (234.5~365.5 kHz)*
RFS, RDS, and RES	: Pseudorandom output streams converted into integer numbers
TN	: Needed number of steps to fulfill the switching frequency
f_{clk}	: Clock frequency
WN	: Needed number of steps to fulfill the duty-ratio
d_L	: Lower duty-ratio limit, (taken 2488)*
EN	: Needed number of steps to fulfill the pulse position
e_L	: Lower pulse position limit, (taken 1500)*
1E4	: For normalizing both of (d_L+RDS) and (e_L+RES) to be a fraction of one, (since their maximum values have been considered as 1E4).

*: For case RRRM, (F_k=234.5~365.5 kHz, d_k=0.249~0.351 and ε_k=0.15~0.56 of T_k).

3. Generating the digital pulse-width modulated waveforms ($V_{gs1,2}$) with the commanded randomization parameters. As shown in Fig. 3, the designed DPWM uses a clocked-counter that increments (up to TN) and resets at the end of every switching cycle of the PWM (see reset1 signal). When the counter value lies between the reference values {EN, EN+WN}, the controller keeps the PWM output state high, else low. In this way, the digital pulse-width modulated waveforms ($V_{gs1,2}$) are generated with the commanded randomization parameters.

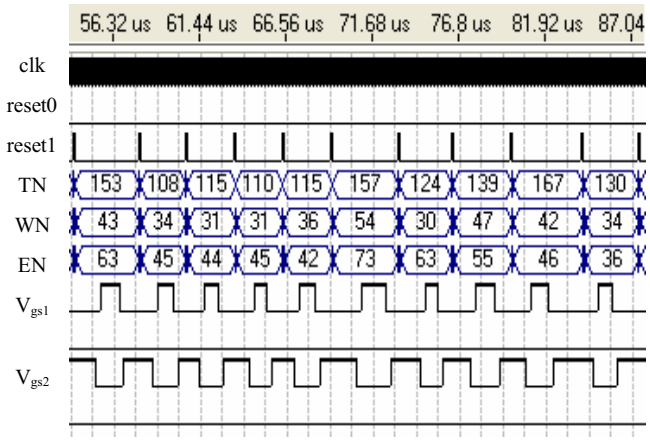


Fig. 3. VHDL simulation of the proposed FPGA-based controller with RRRM scheme.

IV. EXPERIMENTAL VERIFICATION

All the spread-spectrum schemes, described previously, have been designed and implemented using an Altera FPGA. A synchronous buck converter topology has been selected in order to improve efficiency and reduce heat loss. The output inductor and capacitor have been sized such that the converter operates in continuous conduction mode (CCM). Table II illustrates the converter power-circuit parameters.

TABLE II
THE CONVERTER POWER-CIRCUIT PARAMETERS.

Symbol	Description	Value
V_{in}	Input voltage (V)	12
V_o	Output voltage (V)	3.3
I_o	Output current (A)	5
f_{csw}	Center switching frequency (kHz)	300
L	Output inductor (µH)	4.3
C	Output capacitor (µF)	470
C_{in}	Input capacitor (µF)	100

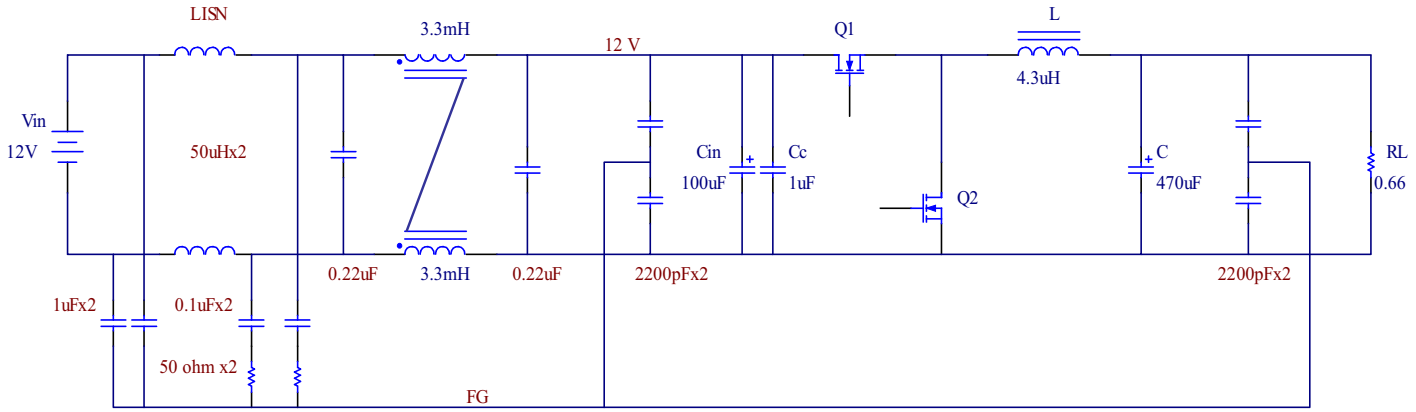


Fig. 4. Experimental circuit for conducted-noise measurements.

The conducted-noise has been measured across the input terminals of the converter using line impedance stabilization networks (LISN), [5]. Fig. 4 describes Experimental circuit for conducted-noise measurements. The LISN is used to standardize the input impedance seen from the converter input and sense the conducted-noise, which is measured by an EMI receiver. Noise measurements have been taken at:
V_{in} = 12 V, V_o = 3.3 V, and I_o = 5 A.

V. RESULTS AND DISCUSSION

Fig. 5 illustrates the measured conducted-noise spectrum of the converter with different spread-spectrum schemes. It is clear that the noise peaks are concentrated in two regions; the first region at the low frequency range (0.15 ~ 1 MHz) around the center switching frequency, and the other region at the high frequency range (1 ~ 30 MHz).

Comparing Fig. 5.(b ~ d) with Fig. 5.(e ~ h) reveals that the switching frequency, as a randomization parameter, is more efficient in spreading the conducted-noise than the duty-ratio or the pulse position parameters.

Fig. 6 presents the effect of the spread-spectrum schemes on the conducted-noise peak reduction at both low and high frequency ranges. This comparison has been carried-out by subtracting the conducted-noise peak of the PWM scheme from that of the spread-spectrum scheme, at both of the two regions. It can be seen that the RCFRPPMFD and RCFMVD schemes achieve a similar performance.

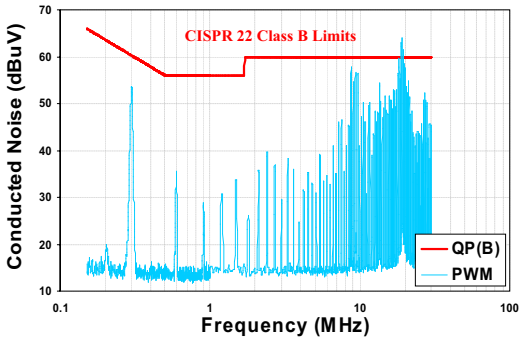
The RPWM scheme gives the worst performance. It poorly improves the conducted-noise spectrum at the high frequency range. Moreover, it increases the conducted-noise peak at the low frequency range. However, the RRRM scheme attains the best performance. It provides the highest conducted-noise peak reduction at the low frequency range. Furthermore, it decreases the conducted-noise peak at the high frequency range by 7.8dB.

VI. CONCLUSIONS

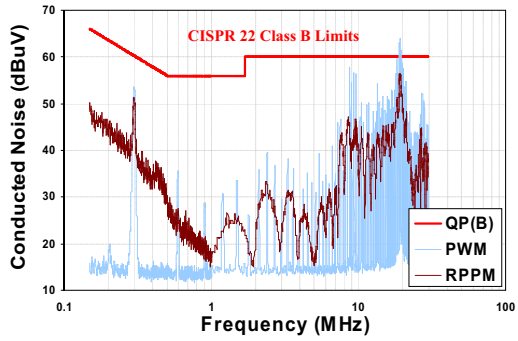
Many spread-spectrum schemes, several of which are new, have been designed and implemented using FPGA for conducted-noise reduction in DC-DC converters. Moreover, the effect of using such schemes on the conducted-noise characteristics of the converter has been experimentally investigated. It can be concluded that:

1. The RPWM scheme gives the worst performance. It poorly improves the conducted-noise spectrum at the high frequency range. Moreover, it increases the conducted-noise peak at the low frequency range.
2. The switching frequency, as a randomization parameter, is more efficient in spreading the conducted-noise than the duty-ratio or the pulse position parameters.
3. The RRRM scheme attains the best performance. It provides the highest conducted-noise peak reduction at the low frequency range. Furthermore, it decreases the conducted-noise peak at the high frequency range by 7.8dB.

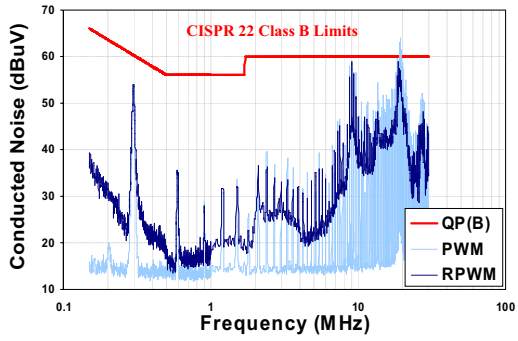
Currently, a detailed study of the RRRM scheme is being carried-out by the authors. It includes calculation/estimation of the noise spectrum, and sweeping the three randomization parameters for reaching the values which achieve the best conducted-noise spectrum spreading.



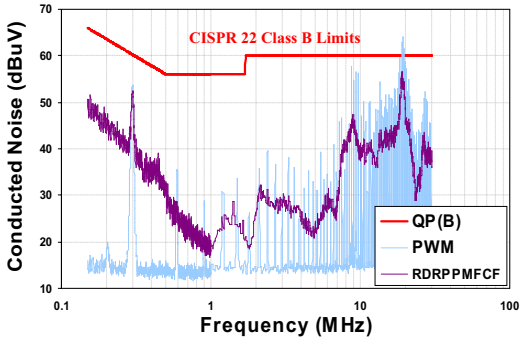
(a) PWM, (F_k=300 kHz, d_k=0.3, and ε_k=0.0).



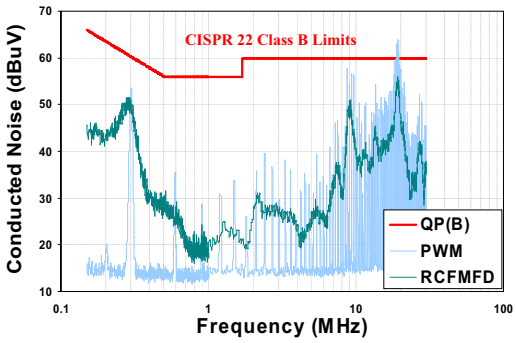
(b) RPPM, (F_k=300 kHz, d_k=0.3, and ε_k=0.15~0.56 of T_k).



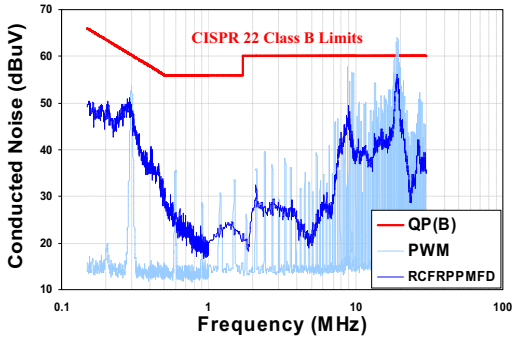
(c) RPWM, (F_k=300 kHz, d_k=0.249~0.351, and ε_k=0.0).



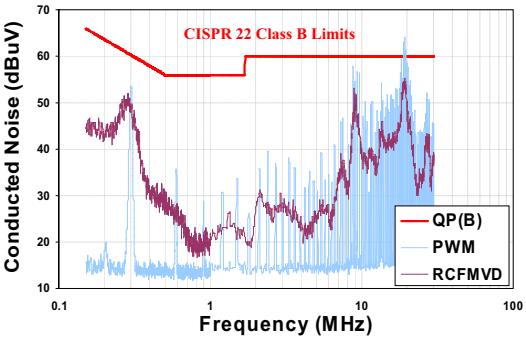
(d) RDRPPMFCF, (F_k=300 kHz, d_k=0.249~0.351, and ε_k=0.15~0.56 of T_k).



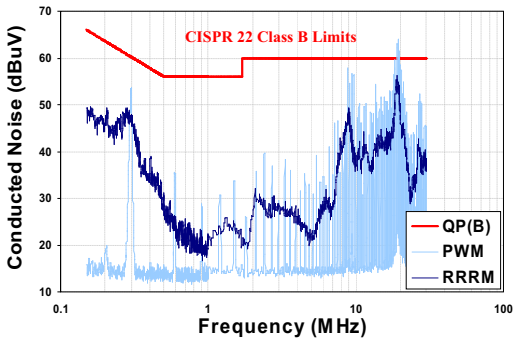
(e) RCFMFD, (F_k=234.5~365.5 kHz, d_k=0.3, and ε_k=0.0).



(f) RCFRPPMFD, (F_k=234.5~365.5 kHz, d_k=0.3, and ε_k=0.15~0.56 of Tk).



(g) RCFMVD, (F_k=234.5~365.5 kHz, d_k=0.249~0.351, and ε_k=0.0).



(h) RRRM, (F_k=234.5~365.5 kHz, d_k=0.249~0.351, and ε_k=0.15~0.56 of T_k).

Fig. 5. The measured conducted-noise spectrum of the converter with different spread-spectrum schemes.

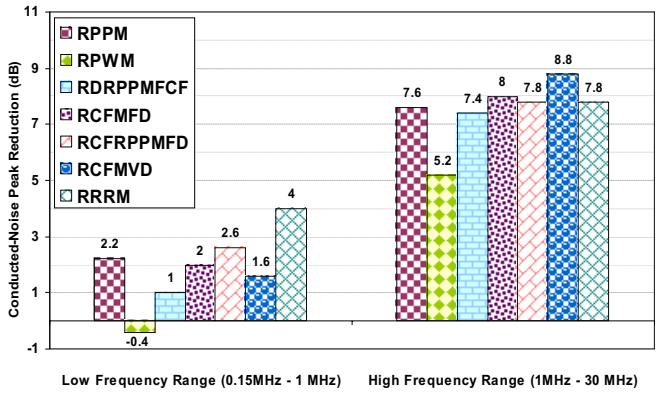


Fig. 6. The effect of the spread-spectrum schemes on the conducted-noise peak reduction.

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