Consideration for Input Current-Ripple of Pulse-link DC-AC Converter for Fuel Cells

Kentaro Fukushima*, Tamotsu Ninomiya†, Masahito Shoyama*,

Isami Norigoe**, Yosuke Harada** and Kenta Tsukakoshi**

* Kyushu University, Fukuoka, Japan, e-mail: *fukushima@ckt.ees.kyushu-u.ac.jp*
† Nagasaki University, Nagasaki, Japan
** EBARA DENSAN, Tokyo, Japan

***Abstract*—This paper mentions the static characteristics of pulse-link DC-AC converter for fuel cells, and considers the input current-ripple reduction method. Fuel cells have weakness about current-ripple because the chemical reaction time is much slower than commercial frequency. Therefore, the input current-ripple reduction is essential factor in the DC-AC converter for fuel cells applications. Input current-ripple from fuel cells gives damage the fuel consumption and life time. The conventional DC-AC converter has large smoothing capacitor between boost converter stage and PWM converter stage, in order to reduce input current-ripple. That capacitor prevents from reduction the size of unit. Authors have proposed a novel topology called as pulse-link DC-AC converter. The pulse-link DC-AC converter topology is no need to insert large capacitor. Furthermore, the series-connected LC circuit between two stages connected in parallel works as ripple canceling. This paper shows the mechanism of current-ripple reduction.**

***Keywords*—DC-AC Converter, Pulse-link, Fuel Cells, Current-Ripple.**

I. BACKGROUND

Environmental issues, such as global heating and energy shortage, have recently become a big international problem. In Japan, about 30% of amount of CO_2 emission is produced by energy conversion department [1]. Therefore, some new clean energy is strongly demanded. One of the new clean energy system using fuel cells has been collecting global interests. When fuel cells generate electricity, a large amount of thermal energy arises at the same time. So, the cogeneration system using both electricity and thermal energy is now researched actively around the world. Especially, a home-use cogeneration system with fuel cells is developed from the stream of what is called distributed power system or micro-grid power systems. Here, the voltage provided by fuel cells is DC, and the power distribution at home is now AC. Therefore, a DC-AC converter is needed for the home-use cogeneration system.

The specifications for DC-AC converter for fuel cells are 3 terms. Firstly, DC-AC converter boosts input voltage from fuel cells to the level of commercial voltage. The voltage from fuel cells is DC, and is generally lower than commercial voltage. Secondly, DC-AC converter has isolation structure between fuel cells stage and load stage from the point of safety. Thirdly, DC-AC converter should reduce input current-ripple. Third-term is special term for fuel cells application. Current-ripple in fuel cells is serious problem. The current-ripple in fuel cells gives damage to the fuel capacity and life span because chemical reaction time is much slower than commercial frequency [2, 3, 4].

In the conventional DC-AC converter for fuel cells, a large smoothing capacitor is inserted in parallel between the boost DC-DC converter and PWM inverter. This capacitor has some rolls. One is to smooth output voltage, another is to reduce input current-ripple. This capacitor absorbs the variation from AC. However, this capacitor disturbs the size reduction of this unit.

To overcome problem, authors has proposed a novel DC-AC converter topology called as Pulse-link DC-AC converter [5, 6]. In this topology, the first-stage boost converter provides a series boosted voltage pulses directly to the second-stage PWM inverter. Therefore, a large capacitor for the smoothed DC power source is not needed. This concept has known as High frequency link or pulse DC link [7, 8]. Furthermore, in order to reduce the current-ripple, a series connected LC circuit is inserted in parallel between two stages.

This paper focuses the mechanism of input current-ripple reduction used by series connected LC circuit. Moreover, the duty ratio of switch is controlled by detecting input current. As the result, input current-ripple is less than 1 Amp.

II. STEADY-STATE ANALYSIS

Fig. 1 shows the proposed circuit topology. As mentioned above, this topology has two stages, and this converter provides boosted pulsed voltage directly to PWM inverter. And between two stages, series LC circuit is connected in parallel in order to reduce current-ripple. The value of the capacitor using this LC circuit is less than the conventional one.

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Fig. 2 shows the switching sequences model of this converter in commercial frequency. This converter has 5 switches. Switch Q_1 controls the boost pulse from input voltage. And, from S_1 to S_4 are PWM inverter switches. S_1 and S_4 are controlled to make output voltage sinusoidal waveform, while S_2 and S_3 are decided the plus/minus of output voltage. And control combination of S_1, S_3 and S_2, S_4 is a pair. Q_1 and S_1/S_4 are synchronous at rising time. As the result, there are three states in one switching period.

A. Operating State1 (Q_1:ON, S_1:ON, S_3:ON)

Fig. 3(a) shows the equivalent circuit of state 1. State equation on state 1 is written as below:

$$\begin{cases} v_{L_1} = V_i - r_{Q_1}\hat{i}_{L_1} - nr_{Q_1}\hat{i}_{L_2} - nr_{Q_1}\hat{i}_{L_o} \\ v_{L_2} = \hat{v}_{C'} - \hat{v}_{C_3} - nr_{Q_1}\hat{i}_{L_1} - n^2 r_{Q_1}\hat{i}_{L_2} - n^2 r_{Q_1}\hat{i}_{L_o} \\ v_{L_o} = \hat{v}_{C'} - \hat{v}_{C_o} - nr_{Q1}\hat{i}_{L_1} + (r_{s1} + r_{s4} - n^2 r_{Q1})\hat{i}_{L_2} - (r_{s1} + r_{s4})\hat{i}_{L_o} \\ i_{C'} = -\hat{i}_{L_2} - \hat{i}_{L_o} \\ i_{C_3} = \hat{i}_{L_2} \\ i_{C_o} = \hat{i}_{L_o} - \dfrac{\hat{v}_{C_o}}{R_o} \end{cases} \quad (1)$$

Where, $C' = \dfrac{C_1 C_2}{C_1 + n^2 C_2}$.

B. Operating State2 (Q_1:ON, S_1:OFF, S_3:ON)

Fig. 3(b) shows the equivalent circuit of state 2. State equation on state 2 is written as below:

$$\begin{cases} v_{L_1} = V_i - r_{Q_1}\hat{i}_{L_1} - nr_{Q_1}\hat{i}_{L_2} \\ v_{L_2} = \hat{v}_{C'} - \hat{v}_{C_3} - nr_{Q_1}\hat{i}_{L_1} - n^2 r_{Q_1}\hat{i}_{L_2} \\ v_{L_o} = -\hat{v}_{C_o} - nr_{Q1} - (r_{s4} + r_{D3})\hat{i}_{L_o} \\ i_{C'} = -\hat{i}_{L_2} \\ i_{C_3} = \hat{i}_{L_2} \\ i_{C_o} = \hat{i}_{L_o} - \dfrac{\hat{v}_{C_o}}{R_o} \end{cases} \quad (2)$$

C. Operating State3 (Q_1:OFF, S_1:OFF, S_3:ON)

Fig. 3(c) shows the equivalent circuit of state 3. In this state, input power is charged C_2 through the diodes of four PWM switches. State equation on state 3 is written as below:

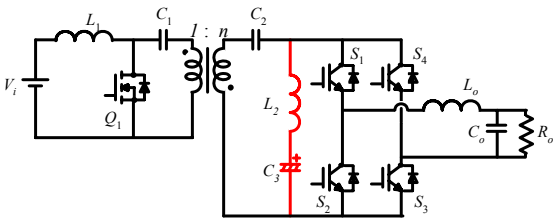


Fig. 1. Pulse-link DC-AC converter topology.

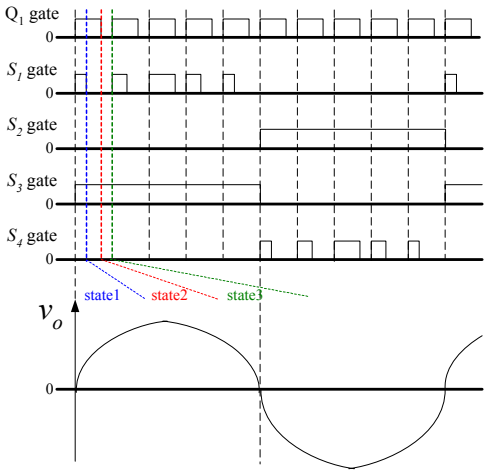
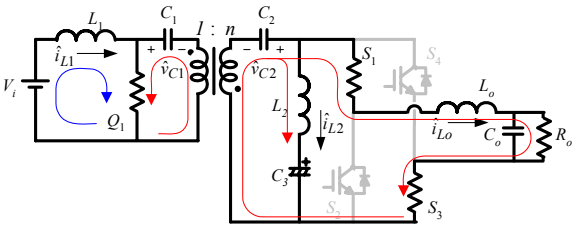
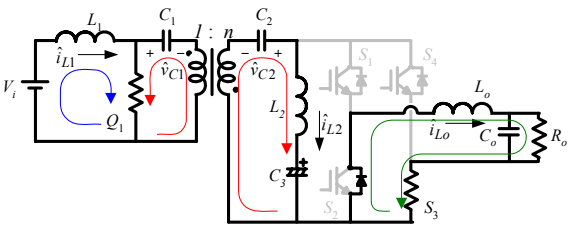


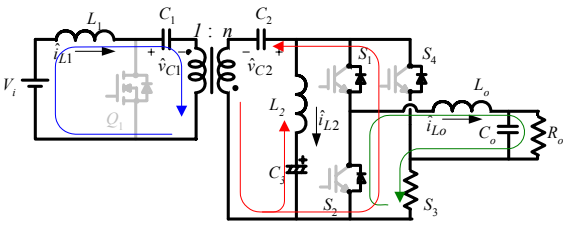
Fig. 2. Switching sequences of the converter.



a. State 1 (Q_1:ON, S_1:ON, S_3:ON).



b. State 2 (Q_1:ON, S_1:OFF, S_3:ON).



c. State 3 (Q_1:OFF, S_1:OFF, S_3:ON).

Fig. 3. Equivalent circuit of each states.

$$
\begin{cases}
v_{L_1} = V_i - \frac{1}{n}\hat{v}_{C'} - \frac{1}{n}(r_{D1'} + r_{D2'})\hat{i}_{L1} - (r_{D1'} + r_{D2'})\hat{i}_{L_2} \\
v_{L_2} = -\hat{v}_{C_3} - \frac{1}{n}(r_{D1'} + r_{D2'})\hat{i}_{L_1} - (r_{D1'} + r_{D2'})\hat{i}_{L_2} - r_{D2'}\hat{i}_{L_o} \\
v_{L_o} = -\hat{v}_{C_o} - \frac{1}{n}r_{D1'}\hat{i}_{L_1} - r_{D2'}\hat{i}_{L_2} - (r_{D2'} + r_{D3'})\hat{i}_{L_o} \\
i_{C'} = \frac{1}{n}\hat{i}_{L_1} - \hat{i}_{L_2} \\
i_{C_3} = \hat{i}_{L_2} \\
i_{C_o} = \hat{i}_{L_o} - \frac{\hat{v}_{C_o}}{R_o}
\end{cases}
\tag{3}
$$

D. Steady State

From above equations, the state-averaging vector is written below by using state space averaging method. Here, on-resistance and conduction losses are neglected.

$$
\frac{dX}{dt} = \begin{bmatrix}
0 & 0 & 0 & -\frac{\frac{1}{n}(1-D_{Q1})}{L_1} & 0 & 0 \\
0 & 0 & 0 & \frac{D_{Q1}}{L_2} & -\frac{1}{L_2} & 0 \\
0 & 0 & 0 & \frac{ds}{L_o} & 0 & -\frac{1}{L_o} \\
\frac{\frac{1}{n}(1-D_{Q1})}{C'} & -\frac{1}{C'} & -\frac{d_s}{C'} & 0 & 0 & 0 \\
0 & \frac{1}{C_3} & 0 & 0 & 0 & 0 \\
0 & 0 & \frac{1}{C_o} & 0 & 0 & -\frac{1}{C_o R_o}
\end{bmatrix} X + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} V_i
\tag{4}
$$

, where $X = \begin{bmatrix} \hat{i}_{L1} & \hat{i}_{L2} & \hat{i}_{Lo} & \hat{v}_{C'} & \hat{v}_{C3} & \hat{v}_{Co} \end{bmatrix}^T$.

From equation (4), the steady-state characteristics are shown below:

$$
V_{c'} = \frac{n}{1-D_{Q1}} V_i \tag{5}
$$

$$
V_o = \frac{n d_s(t)}{1-D_{Q1}} V_i \tag{6}
$$

$$
I_{L1} = \frac{{d_s}^2}{R_o (1-D_{Q1})^2} V_i \tag{7}
$$

Furthermore, from Equation (5), the peak voltage pulse that is input to PWM inverter (v_{inv_in}) is written below

$$
v_{inv\_in} = \frac{n}{1-D_{Q1}} V_i \tag{8}
$$

Here, D_{Q1} is duty ratio of switch Q_1. And, $d_s(t)$ is duty ratio of PWM inverter switch of S_1/S_4. $d_s(t)$ is changed shown as equation (9) in order to make output voltage to be sinusoidal waveforms.

$$
d_s(t) = d_{s1\_\max} \cdot \left| \sin(2\pi \cdot 50t) \right| \tag{9}
$$

TABLE I.
CIRCUIT PAPAREMTER VALUES

Symbol	Description	value
Vi	Input voltage	20[V]
L1	Input inductance	400[uH]
L2	Middle inductance	1[mH]
LM	Magnetizing inductance	400[uH]
C1	primary-side capacitance	3[mF]
C2	Secondary-side capacitance	330[uF]
C3	Middle capacitance	300[uF]
n	Turn ratio	3
Lo	Output inductance	3[mH]
Co	Outout capacitance	9.4[uF]
fs	Switching frequency	30[kHz]

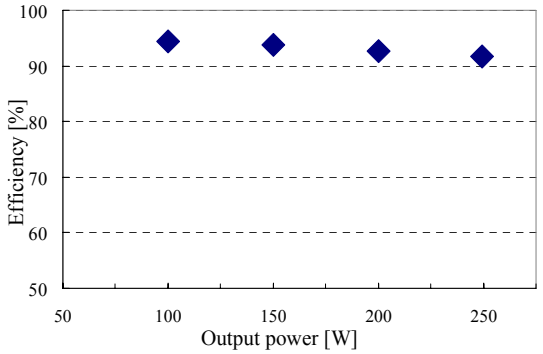


Fig. 4. Characteristics of Efficiency vs. Output power.

Moreover, the relationship of D_{Q1} and $d_{s\_\max}$ is limited Equation (10), because PWM inverter is provided voltage only when Q_1 is ON.

$$
D_{Q1} \geq d_{s1\_\max} \tag{10}
$$

From this limit, pulse output voltage is regarded as constant voltage viewing from PWM inverter.

III. EXPERIMENTAL RESULTS

A. Circuit parameter values

To evaluate the performance of the circuit, the experimental circuit is implemented with the specifications and parameters in Table I. From table I, C_1 is 3[mF], and it is aluminum electrolytic capacitor. C_1 is decided from the allowable current. Primary-side is flown large current, so capacitance of C_1 becomes large value. However, primary-side is low voltage, so the size of aluminum electrolytic capacitor is not so large even if the value is large because withstand-voltage is low. Therefore, large value of aluminum electrolytic capacitor is used at C_1 in this experiment.

B. Characteristics of Efficiency

Fig. 4 shows the characteristics of efficiency vs. output power. Here, it is measured when output voltage is regulated $100 \pm 1[\mathrm{V_{rms}}]$. From fig. 4, it is considered that the efficiency is more than 90 [%]. This topology can convert DC to AC with high efficiency.

C. Waveforms of output voltage and input current

Fig. 5 shows the experimental waveforms of output voltage (v_o), input current (i_i), and inductor current of L_2 (i_{L2}) when output power is 100[W]. And table II shows the experimental measurement. From those results, it is considered that output voltage is achieved to output commercial voltage. Furthermore, it is considered that inductor current of i_{L2} oscillates low frequently with zero crossing.

IV. Input Current-Ripple

Steady-state equation of inductor current of L_2 is equation (7), and shown below, again.

$$I_{L1} = \frac{d_s^{\,2}}{R_o\left(1-D_{Q1}\right)^2} V_i$$

When substitutes equation (9) for above equation, I_{L2} is written below:

$$I_{L1} = \frac{d_{s\_\max}^{\,2}\left(1-\cos\left(2\pi \cdot 100t\right)\right)}{2R_o\left(1-D_{Q1}\right)^2} V_i \qquad (11)$$

Input current is equal to I_{L1}. From this equation, it is considered that input current oscillates low frequency as double commercial frequency.

For the comparison, the experimental waveforms when series L_2C_3 circuit is not inserted are shown in fig. 6. The output load condition is same. When L_2C_3 circuit is not inserted in the topology, input current-ripple is 6.11[A_{p_p}]. On the other hand, in the case when L_2C_3 circuit is inserted, input current-ripple is reduced at 4[A_{p_p}] from fig. 5. And it is sure that efficiency is not depended whether series L_2C_3 circuit or not. From the result, it is considered that series L_2C_3 circuit is effective about input current-ripple reduction. However, it is not enough to reduce input current ripple. Here is mentioned reduction methods of input current- ripple.

A. Optimization of the series L_2C_3 circuit parameter values

Input current-ripple is occurred by output commercial frequency of output voltage. If the resonant frequency of series L_2C_3 circuit connected the circuit in parallel is synchronized 100[Hz], input current-ripple will be reduced. Impedance of series L_2C_3 circuit is written below equation:

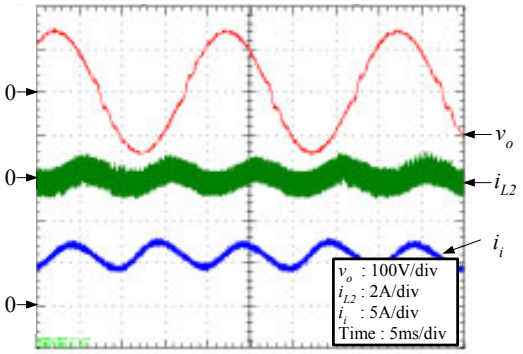


Fig. 5. Experimental waveforms of v_o, i_i, and i_{L2}.

TABLE II.
EXPERIMENTAL MEASUREMENT AT P_o=100[W]

Symbol	Description	value
Vi	Input voltage	20[V]
Ii	Input current	5.3[A]
Vo	Output voltage	100[V(rms)]
P_o	Output resistance	100[W]
η	Efficiency	94[%]

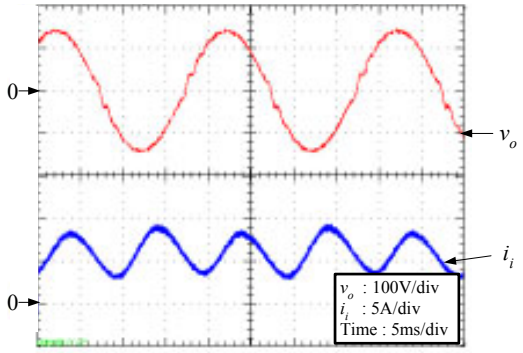


Fig. 6. Experimental waveforms of v_o, and i_i (without L_2C_3).

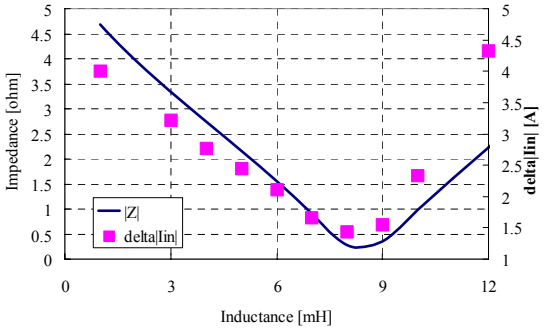


Fig. 7. Inductance values vs. Impedance and Current-ripple.

$$|Z| = \left| j\left(\omega L - \frac{1}{\omega C}\right)\right| \quad (12)$$

Here, inductance is being changed because capacitor is not recommended large capacitance value.

Fig. 7 shows the characteristics of series L_2C_3 impedance and input current-ripple measurement by changing of L_2. Here, the value of C_3 is 300[uF], and $\omega = 2 \cdot \pi \cdot 100$ [rad/s]. From fig. 8, it is considered that impedance |Z| curve and experimental measurement of input current-ripple is agreed well.

Furthermore, the experimental waveforms at L_2=8[mH] is shown in Fig. 8. From Fig. 8, inductor current of L_2 is oscillated with opposite phase of output semi-sinusoidal voltage. This thing means that when output load is light, extra energy from input power is stored by series L_2C_3, and when output power is heavy, series L_2C_3 provides with input power. From the result, this series L_2C_3 circuit is regarded as pulse energy tank, and works as ripple canceling circuit.

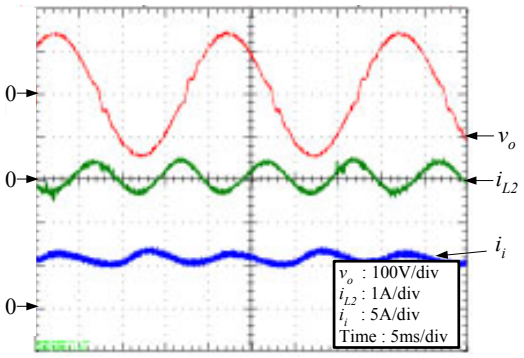


Fig. 8. Experimental waveforms of v_o, i_i, and i_{L2} (L_2=8mH).

B. *Sensed current and controlled duty ratio of switch*

To reduce input-current-ripple further, D_{Q1} is controlled by detecting input current. In the experiment, FPGA is used and it controls with A/D converter shown Fig. 9. In the experiment, current sensor detects input current. 1[A] is converted to 0.125[V] used by current sensor. And the converted voltage is input to A/D converter. 0.01[V] is corresponding to 1 binary data at A/D converter. The duty ratio signal of switch Q_1 ($Q_{1signal}$) which is binary data is calculated by below equation:

$$Q_{1signal} = Q_{1signa\_ref} + k\left(I_{in} - I_{ref}\right) \quad (13)$$

, where $Q_{1signal\_ref}$ is corresponding to the binary data that duty ratio of switch Q_1 (D_{Q1}) is 0.7, and I_{ref} is converted reference input current to binary data.

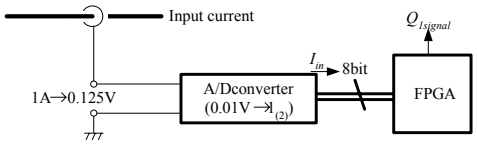


Fig. 9. Current sensing component block.

Fig. 10 shows the experimental waveforms of output v_o, i_i, and i_{L2} when D_{Q1} is controlled by detecting input current. From fig. 10, it is observed that input current i_i is almost canceled the low frequency ripple. Ripple is less than 1[A].

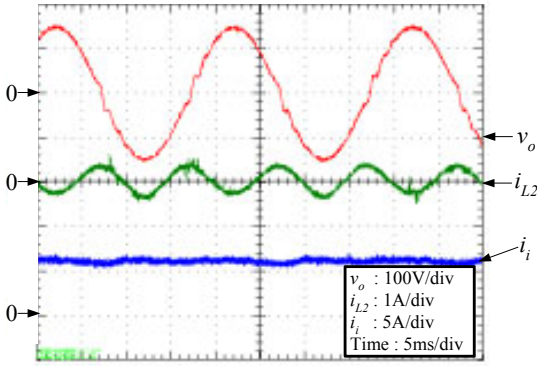


Fig. 10. Experimental waveforms of v_o, i_i, and i_{L2}.
(with input current sensed)

V. CONCLUSION

This paper analyzed Pulse-link DC-AC converter for fuel cells and considered input current-ripple. This converter provides the boosted voltage pulses directly to the PWM inverter, and L_2 and C_3 circuit is inserted to reduce input-current ripple. This topology converts DC to AC with high efficiency. Furthermore, the mechanism of input current-ripple is cleared and input current-ripple reduction methods are shown. Input current-ripple is caused by commercial frequency.

Series L_2 and C_3 circuit works as current ripple canceling if parameters are optimized as resonant condition. Moreover, the method which is sensed input current of this converter and controlled D_{Q1} is shown to cancel input-current ripple. When the control is worked, the input-current ripple is improved to be reduced less than 1[A].

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