Optimal Bus Capacitance Design for System Stability in On-Board Distributed Power Architecture

Seiya Abe[*] , Masahiko Hirokawa[**], Masahito Shoyama[*] and Tamotsu Ninomiya[***]
[*] Kyushu University, 744, Motooka, Nishi-ku, Fukuoka, 819-0395, Japan
[**]TDK Corporation, 2-15-7, Higashi-Ohwada, Ichikawa, Chiba, 272-8558, Japan
[***]Nagasaki University, 1-14, Bunkyo-Machi, Nagasaki, 852-8521, Japan

***Abstract*— Recently, the distributed power system is mainly used for the power supply system which requires the low-voltage / high-current output. The distributed power system consists of bus converter and POL. The most important factor is the system stability in bus architecture design. The overlap between the output impedance of bus converter and input impedance of POL causes system instability, and it has been an actual problem. Increasing the bus capacitor, system stability can be reduced easily. However, due to the limited space on the system board, increasing of bus capacitors is impractical. The urgent solution of the issue is desired strongly. This paper presents the output impedance design for on-board distributed power system by means of three control schemes of bus converter. The output impedance peak of the bus converter and the input impedance of the POL are analyzed, and it is conformed by experimentally for stability criterion. Furthermore, the optimal intermediate bus capacitance design for system stability is proposed.**

***Keywords*— Distributed power system, bus converter design, output impedance, intermediate bus capacitance.**

I. INTRODUCTION

Various LSI is used in the telecommunication application equipments and the driving voltage is various. On the other hand, increase of load current is also remarkable by advanced function of LSI. Since the present LSI is designed in accordance with semiconductor manufacture technology, the tolerance level of operation voltage is very narrow. Consequently, the voltage drop by the wiring impedance of power line causes malfunction of LSI. In order to reduce the malfunction of LSI by the voltage drop, it is proposed that the converter is arranging very close to the LSI. This converter is called POL. Thus, the power supply system which requires the low-voltage / high-current output has been changing from conventional centralized power system to distributed power system. The distributed power system consists of first-stage isolated DC-DC converter as a bus converter and second-stage non-isolated DC-DC converter as a POL. However, the instability phenomenon in a distributed power system is posing a problem recently. This is instability phenomenon resulting from overlapping between the output impedance of bus converter and the input impedance of POL. Increasing the bus capacitor, system stability can be reduced easily. However, due to the limited space on the system board, increasing of bus capacitors is impractical. The urgent solution of the issue is desired strongly, and the various discussion of system stability has been reported[1-8]. Then, we also have reported the detailed discussion of system stability by control schemes of bus converter (Un-regulated, Semi-regulated and Full-regulated)[9-14]. However, so far, the detailed discussion of practical design and the optimal intermediate bus capacitance design of bus converter about on-board distributed power system has not been reported. This paper presents the optimal design of bus converter for on-board distributed power system by means of three control schemes of bus converter.

II. DISCRIMINATION OF STABILITY

Figure 1 shows the distributed power system consisting of bus converter and POL. Even if each converter has stable operation, the instability phenomenon may occur by connecting two converters in series. Bus converter and POL have input-to-output voltage transfer function Gvb(s) and Gvp(s), respectively. The overall input-to-output voltage transfer function Gvv(s) is given following equation;

$$G_{vv}(s) = \frac{G_{vb}(s)G_{vp}(s)}{1 + Z_o(s)/Z_{in}(s)} \quad (1)$$

where Zo (s) is the output impedance of bus converter, and Zin(s) is the input impedance of POL. From Eq. (1), the input and output impedance is greatly concerned with the system stability. The stability of closed-loop system is decided with the characteristics equation 1+Zo(s)/Zin(s). This means relation between Zo(s) and Zin(s) decides the system stability. This system may become unstable when both impedances are overlapped, as shown in Fig. 2 (a). It is necessary to eliminate this impedance overlap for system stability. However, eliminating this impedance overlap for all frequency range is very difficult.

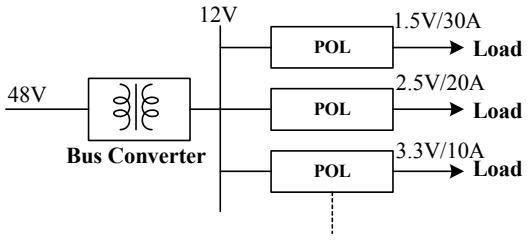


Fig. 1. On-board distributed power system.

978-1-4244-1742-1/08/$25.00 ©

On the other hand, it may have stable operation even if both impedances are overlapped. This is because the phase margin becomes large under the influence of the input impedance. When the bandwidth of POL is enough wider than the bandwidth of bus converter, if the peak value of output impedance becomes almost equal to the steady-state value of input impedance |Zin(0)| as shown in Fig. 2 (b), then this system becomes stability limit as shown in Fig. 2 (b). Moreover, this system becomes unstable if the peak value of output impedance exceeds |Zin(0)|. From mentioned above consideration, the new stability criterion can be defined as follows[15].

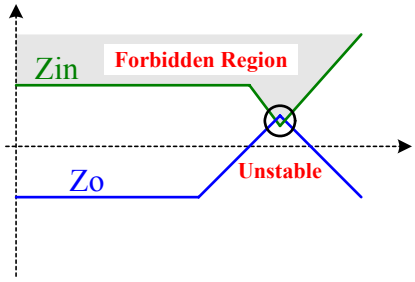
$$\begin{cases} |Z_{in}(0)| \geq Z_{o\_peak} & : \ Stable \\ |Z_{in}(0)| < Z_{o\_peak} & : \ Unstable \end{cases}$$

III. IMPEDANCE ANALYSIS

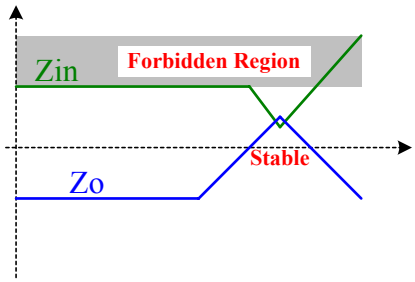
The half-bridge converter with the most popular circuit of the power-stage is used as a bus converter, and the synchronous buck converter with the most popular circuit is used as POL. Figure 3 and 4 show the circuit diagrams, respectively. The output impedance of bus converter and the input impedance of POL can be derived by applying the stage space averaging method[16,17].

A. Input Impedance

At first, the low-frequency value |Zin(0)| of input impedance is estimated. The input impedance of POL can be derived as following equation[18].



(a) Conventional discrimination.



(b) New discrimination.

Fig. 2. Stability discrimination.

$$\frac{1}{Z_{in}(s)} = \frac{1}{Z_N(s)} \cdot \frac{T_p(s)}{1+T_p(s)} + \frac{1}{Z_D(s)} \cdot \frac{1}{1+T_p(s)} \quad (2)$$

From Eq. (2), the low-frequency value of input impedance |Zin(0)| is given by following equation.

$$\left|Z_{in}(0)\right|_{(dB\Omega)} \approx 20\log\left(\frac{R+r_L}{D^2}\right) \quad (dB\Omega) \quad (3)$$

|Zin(0)| has minimum value at rated load, so the estimation of |Zin(0)| must be at rated load. Next, the output impedance is examined.

B. Output Impendance

The output impedance of bus converter can be derived as following equations.

Open loop

$$Z_o(s) = \frac{s^2 L_b C_b r_{c_b} + s\left(L_b + C_b r_{L_b} r_{c_b}\right) + r_{L_b}}{s^2 L_b C_b + s C_b \left(r_{L_b} + r_{c_b}\right) + 1} \quad (4)$$

Closed loop

$$Z_{oc}(s) = \frac{Z_o(s)}{1+T_b(s)} \quad (5)$$

where,

$$T_b(s) = k \cdot PWM \cdot G_{dv_b}(s) \quad (6)$$

$$G_{dv_b}(s) = \frac{V_s}{P_b(s)}\left(sC_b r_{c_b} + 1\right) \quad (\text{Vs=Vin/2n}) \quad (7)$$

$$P_b(s) = s^2 L_b C_b + s C_b \left(r_{L_b} + r_{c_b}\right) + 1 \quad (8)$$

k : sense gain products error amp. gain,

PWM : gain of the comparator.

In open loop case, the peak frequency is the same resonant frequency fp of the loop gain T(s) as shown in Fig. 5, and the peak value of the output impedance can be derived from Eq. (4).

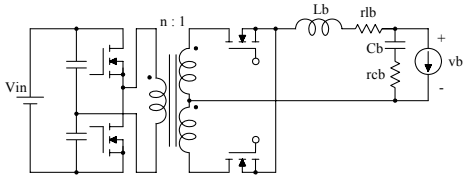


Fig. 3. Bus converter.

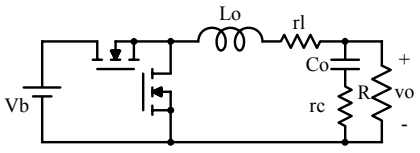


Fig. 4. Point of Load.

$$Z_{o\_peak} = \frac{L_b}{C_b\left(r_{c_b} + r_{L_b}\right)} \quad (9)$$

In closed loop case, the output impedance peak moves to crossover frequency fc as shown in Fig. 5. In this instant the peak value of the closed loop output impedance can be derive following equation.

$$Z_{oc\_peak} = \frac{L_b}{C_b\left\{\left(1+\alpha\right)r_{c_b} + r_{L_b}\right\}} \quad (10)$$

where,

$$\alpha = \left|T(0)\right| = k \cdot PWM \cdot V_s \quad (11)$$

Moreover, from transfer function of loop gain, the crossover frequency fc is expressed as follows by means of peak frequency fp of loop gain.

$$f_c = \sqrt{1+\alpha}\, f_p \quad (12)$$

From Eq. (10) (12), the peak value of closed loop output impedance is expressed as follows.

$$Z_{oc\_peak} = \frac{L_b}{C_b\left\{\left(\frac{f_c}{f_p}\right)^2 r_{C_b} + r_{L_b}\right\}} \quad (13)$$

As shown in Eq. (13), if fc is equal to fp, it becomes the same as Eq(9). Therefore, the peak value of output impedance is calculable by means of Eq. (13).

IV. OUTPUT IMPEDANCE SPECIFICATION

The output impedance characteristic of each control shames is different, and each bus converter has different operation. Therefore, the output impedance design suitable for the feature of each control method is required. From now, the output impedance design for each control shames is considered.

A. Un-regulated

In un-regulated case, the output impedance is the same as open-loop output impedance because of this control method has no control loop. In order to reduce the peak value of output impedance, it is effective to make inductance small or to enlarge capacitance.

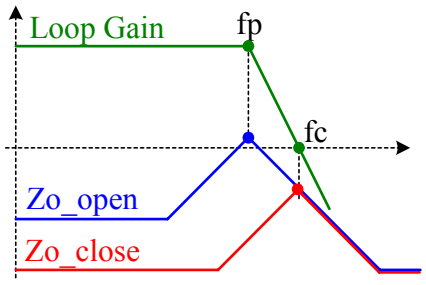


Fig. 5. Output impedance peak.

Generally, un-regulated bus converter is operated at maximum duty ratio. Therefore, the inductor of the bus converter can be reduced as small as possible to reduce the system instability. The peak value of output impedance is reducing with small inductor. Figure 6 shows the experimental result of the relation between the output impedance and inductance. Moreover, Fig. 7 shows the analytical and experimental results of the relation between the peak value of output impedance and inductance. Both results agreed well. As mentioned above, the peak of impedance is easily obtained from Eq. (13). However, this method depends on converter topology that has a double-ended circuit at secondary side such as half-bridge or full-bridge. Moreover, there are some limits such that high accurate input voltage or a POL with wide input range.

B. Semi-regulated

Semi-regulated bus converter has a control loop. However, regulation is related to variation of input voltage, therefore the output impedance is same as un-regulated case. In this case, the duty ratio is changed, and the inductor of the bus converter cannot be reduced. Therefore, very large bus capacitor is needed to reduce the peak value of output impedance.

Figure 8 shows the experimental result of the relation between the output impedance and capacitance. Moreover, Fig. 9 shows the analytical and experimental results of the relation between the peak value of output impedance and capacitance. Both results agreed well.

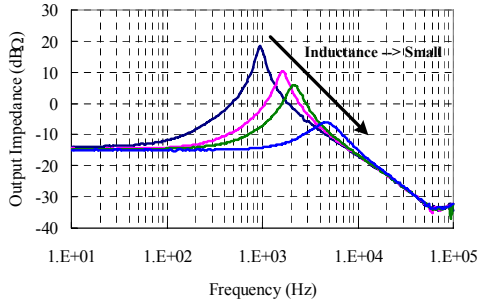


Fig. 6. Inductance and output impedance.

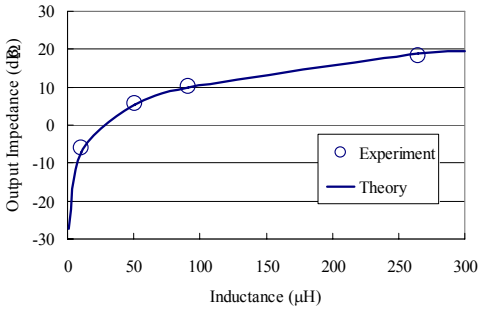


Fig. 7. Inductance and peak value of Zo.

In semi-regulated case, essentially it becomes very unstable and we have found that the demerit is very large capacitors are needed at the intermediate bus in order to be stable. However, it can be used at limited conditions such as wide input range (36-75V) and POL with low power (in other words, POL with very high input impedance).

C. *Full-regulated*

Full-regulated bus converter has a feedback loop, so the output impedance characteristic is changed. Therefore, output impedance can be made small with wide bandwidth. Figure 10 shows the experimental result of the relation between the output impedance and bandwidth. Moreover, Fig. 11 shows the analytical and experimental results of the relation between the peak value of output impedance and bandwidth. Both results agreed well.

Next, the relation between capacitance and output impedance peak is examined in closed loop case.

In closed loop case, if capacitance Cb changes to Cb+Cadd, peak frequency fp of loop gain is changed as follows.

$$f_p' = \frac{1}{2\pi\sqrt{L_b\left(C_b + C_{add}\right)}} \quad (14)$$

Therefore, the crossover frequency fc is changed as follows.

$$f_c' = \sqrt{1+\alpha}\, f_p' \quad (15)$$

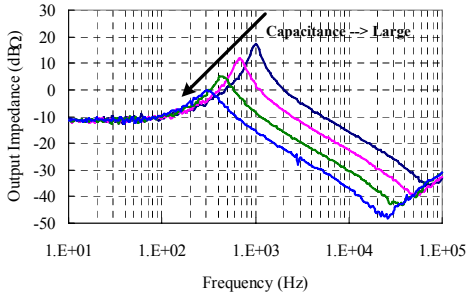


Fig. 8. Capacitance and output impedance.

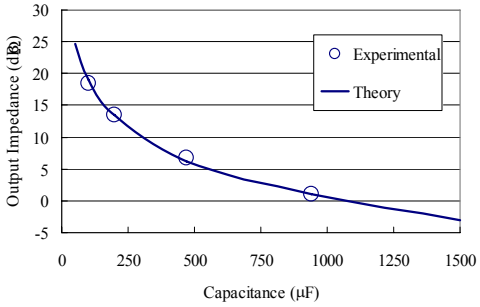


Fig. 9. Capacitance and peak value of Zo.

Moreover, frequency ratio fc'/fp' is given as following equation.

$$\frac{f_c'}{f_p'} = \frac{f_c}{f_p} \quad (16)$$

From these results, output impedance peak can be expressed as following equation.

$$Z_{oc\_peak}' = \frac{k_{esr} C_b}{\left(C_b + C_{add}\right)} Z_{oc\_peak} \quad (17)$$

where, k

$$k_{esr} = \frac{(1+\alpha) r_{cb} + r_{Lb}}{(1+\alpha) r_{cb}' + r_{Lb}} \quad (18)$$

Figure 12 shows the experimental result of the relation between the output impedance and capacitance in closed loop case. Moreover, Fig. 13 shows the analytical and experimental results of the relation between the peak value of output impedance and capacitance in closed loop case. Both results agreed well. In this case, the total ESR is greatly changed by the additional capacitor. Moreover, in the case of closed loop, ESR has a great influence to the output impedance peak. Therefore, estimation of ESR is very important.

V. Optimal Design of Bus Converter

In order to evaluate the performance of this system, the experiment circuits are implemented using the specifications and parameters in Table 1.

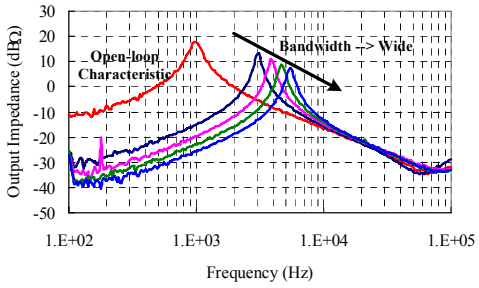


Fig. 10. Bandwidth and output impedance.

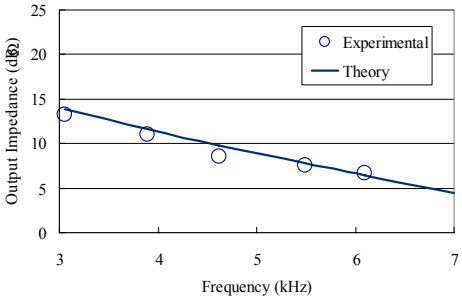


Fig. 11. Bandwidth and peak value of Zo

Here, the case with two POLs is discussed for actual example. The practical design process is shown below.

A. Input impedance estimation

The low-frequency value |Zin(0)| of input impedance is given by Eq. (3). The duty ratio is D=0.275 and output resistance is R=0.66(Ω) from the relation input and output. In this case, the |Zin(0)| is 20.6(dBΩ).

When two POLs of same condition are connecting in parallel, |Zin(0)| is 14.6(dBΩ). Figure 14 shows the experimental result of input impedance. The low-frequency value |Zin(0)| is around 15(dBΩ) as shown in Fig. 14.

The experimental results and analytical results are agreed well. If the stability margin is set to 6(dBΩ), then the peak value of output impedance must be set to 8.6(dBΩ).

B. Output impedance design

Figure 15 shows the output impedance characteristic of the basic case using the parameter of Table 1. As shown in Fig. 15, the peak value of the output impedance is around 18(dBΩ). From mentioned above calculation, the peak value of the output impedance needs to set around 8.6(dBΩ) for sufficient system stability.

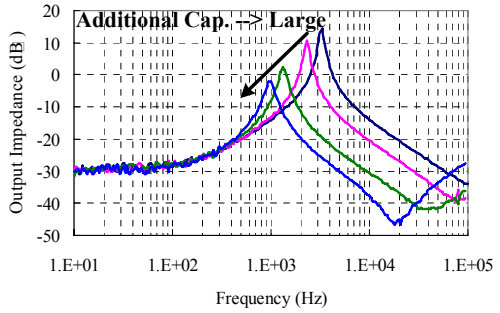


Fig. 12. Additional capacitance and output impedance

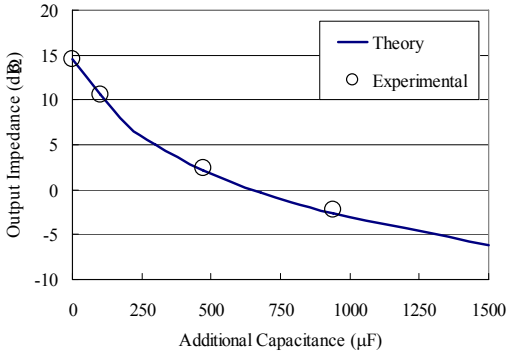


Fig. 13. Additional capacitance and peak value of Zo

TABLE I. CIRCUIT PARAMETERS

	Symbol	Description	Value
Bus Converter	Vin	Input Volotage	48V
	Vb	Bus Volotage	12V
	Lb	Output Inductor of Bus Converter	270μH
	Cb	Output Capacitor of Bus Converter	100μF
	rlb	Registance of Lb	300mΩ
	rcb	ESR of Cb	25mΩ
	kb	Feedback gain (with sence gain)	0.9
POL	Vo/Io	Output Condition	3.3V/5A
	Lo	Output inductor	2.8μH
	Co	Output capacitor	820μF
	rl	Registance of Lo	25mΩ
	rc	ESR of Co	10mΩ

In un-regulated case, the optimal inductance value is considered because the stability is improved by small inductance. From Eq. (13), the optimal inductance value can be derived as following equation.

$$L_{b\_optimal} = C_b\left(r_{C_b} + r_{L_b}\right)Z_{o\_peak} \quad (19)$$

where, the unit of |Zo_peak| is Ω.

Since the output impedance must be set to 8.6(dBΩ), the inductance value is set to around 87(μH) from Eq. (19). Figure 16 shows the experimental result of the output impedance with small inductance.

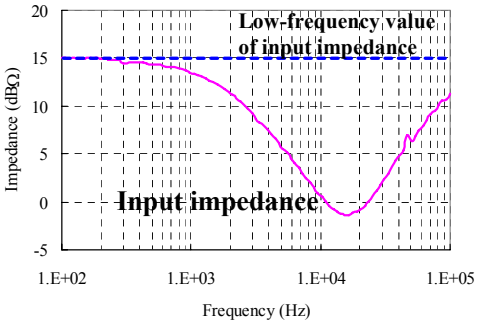


Fig. 14. Input impedance characteristic.

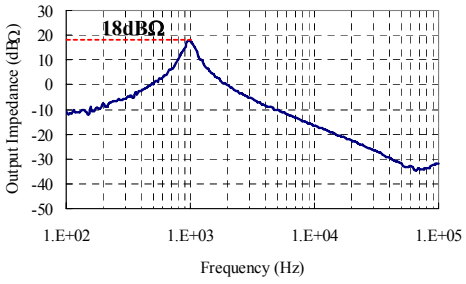


Fig. 15. Output impedance (Basic parameters).

The inductance value is around 90 (μH), and the peak value of output impedance is around 8.5 (dBΩ). The experimental results and analytical results are agreed well. Moreover, in open loop case, since the rL is generally larger than rc, the output impedance does not become smaller than rL as shown in Fig. 6. Therefore, the inductance value has minimum value. From Eq. (19), the minimum value of the inductance is given by following equation.

$$L_{b\_\min} = C_b\left(r_{C_b} + r_{L_b}\right)r_{L_b} \quad (20)$$

In this case, the minimum value of inductance is around 10 (μH).

In semi-regulated case, the optimal capacitance value is considered because the stability is improved by large capacitance. From Eq. (13), the optimal capacitance value can be derived as following equation.

$$C_{b\_optimal} = \frac{L_b}{\left(r_{C_b} + r_{L_b}\right)Z_{o\_peak}} \quad (21)$$

where, the unit of |Zo_peak| is Ω.
Since the output impedance must be set to 8.6(dBΩ), the capacitance value is set to around 300(μF) from Eq. (16). In this case, the influence of ESR is considered. Because the ESR becomes small when the capacitor is connected in parallel.

Figure 17 shows the experimental result of output impedance with large capacitance. The capacitance value is 300 (μF), and the peak value of output impedance is around 8 (dBΩ). The experimental results and analytical results are agreed well.

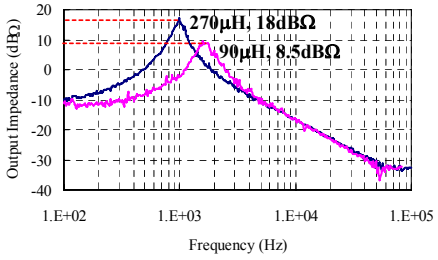


Fig. 16. Output impedance with small inductor.

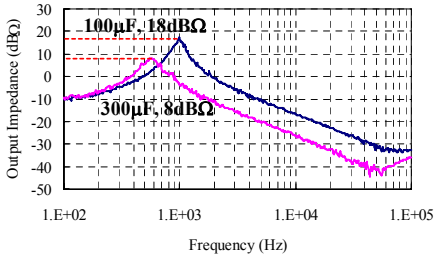


Fig. 17. Output impedance with large capacitor.

Moreover, the output impedance does not become smaller than rL as shown in Fig. 8. Therefore, the capacitance value has maximum value. From Eq. (21), the maximum value of the capacitance is given by following equation.

$$C_{b\_\max} = \frac{L_b}{\left(r_{C_b} + r_{L_b}\right)r_{L_b}} \quad (22)$$

In this case, the maximum value of capacitance is around 2.8 (mF).

In full-regulated case, the optimal bandwidth is considered because the stability is improved by wide bandwidth. From Eq. (13), the optimal bandwidth can be derived as following equation.

$$f_{c\_optimal} = f_p\sqrt{\frac{\frac{L_b}{C_b Z_{oc\_peak}} - r_{L_b}}{r_{C_b}}} \quad (23)$$

where, the unit of |Zo_peak| is Ω.
Since the output impedance must be set to 8.6(dBΩ), the bandwidth is set to around 5.1kHz from Eq. (23). Figure 18 shows the experimental result of the output impedance with wide bandwidth. The bandwidth is around4.7kHz, and the peak value of output impedance is around 8.5 (dBΩ). The experimental results and analytical results are agreed well.

Next, the optimal capacitance is considered in closed loop case. From Eq. (17), the optimal additional capacitance can be derived as following equation.

$$C_{add\_optimal} = \left(\frac{k_{esr}Z_{oc\_peak}}{Z_{oc\_peak}'} - 1\right)C_b \quad (24)$$

The basic parameters case, the closed loop output impedance peak is around 14.5(dBΩ). Since the output impedance must be set to 8.6(dBΩ), the additional capacitance is set to around 150μF from Eq. (24). Figure 19 shows the experimental result of the output impedance with additional capacitance. The capacitance is around 150μF, and the peak value of output impedance is around 9 (dBΩ). The experimental results and analytical results are agreed well.

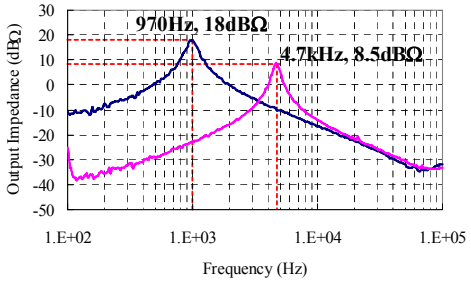


Fig. 18. Output impedance with wide bandwidth.

VI. CONCLUSIONS

This paper presents the output impedance design for on-board distributed power system by means of three control methods of bus converter. The output impedance peak of the bus converter and the input impedance of the POL were analyzed, and it was conformed by experimentally for stability criterion. As a result, the standard of the discrimination of stability on a frequency response of input and output impedance was clarified. Furthermore, the design process of each control method for system stability was proposed.

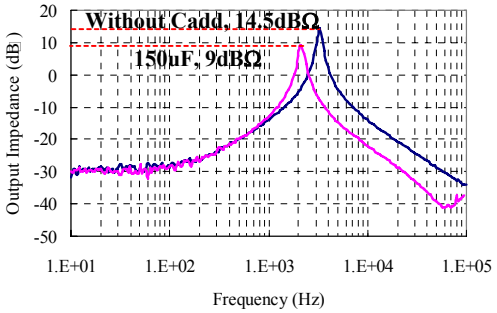


Fig. 19. Output impedance with additional capacitance

REFERENCES

[1] C. M. Wildrick, F. C. Lee, B. H. Cho, B. Choi, "A Method of Defining the Load Impedance Specification for A Stable Distributed Power System", IEEE Transactions on Power Electronics Vol. 10. No. 3. May 1995, pp. 280-284.

[2] X. Feng, Z. Ye, K. Xing, F. C. Lee, D. Borojevic, "Individual Load Impedance Specification for a Stable DC Distributed Power System", IEEE Applied Power Electronics Conference (APEC) 1999, pp. 923-929.

[3] X. Feng, F. C. Lee, "On-line Measurement on Stability Margin of DC Distributed Power System", IEEE Applied Power Electronics Conference (APEC) 2000, pp. 1190-1196.

[4] M. P. Sayani, J. Wanes, " Analyzing and Determining Optimum On-Board Power Architectures for 48V-input Systems", IEEE Applied Power Electronics Conference (APEC) 2003.

[5] K. Hisanaga, K. Harada, "Stability Analysis of the Distributed Power System with Intermediate Bus Converter", IEICE Technical Report, Vol.103, No.199, pp.19-24, Jul. 2003 (in Japanese).

[6] K. Hisanaga, K. Harada, "Stability Analysis of the Distributed Power System with Intermediate Bus Converter (2nd Report)", IEICE Technical Report, Vol.103, No.652, pp.7-12, Feb. 2004 (in Japanese).

[7] Y. Ren, M. Xu, K. Yao, Y. Meng, F. C. Lee, J. Guo, "Two-Stage Approach for 12V VR", IEEE Applied Power Electronics Conference (APEC) 2004.

[8] J. Wei, F. C. Lee, "An Output Impedance-Based Design of Voltage Regulator Output Capacitors for High Slew-Rate Load Current Transients", IEEE Applied Power Electronics Conference (APEC) 2004.

[9] B. Choi, D. Kim, D. Lee, S. Choi, J. Sun, "Analysis of Input Filter Interactions in Switching Power Converters", IEEE Transactions on Power Electronics, Vol. 22, No. 2, March 2007, pp. 452-460.

[10] S. Abe, M. Hirokawa, T. Zaitsu, T. Ninomiya, "Stability Design of Bus Converter Following by POLs in Distributed Power System", IASTED Circuits, Signals,and Systems (CSS), 2005, pp552-557.

[11] S. Abe, H. Nakagawa, M. Hirokawa, T. Zaitsu , T. Ninomiya, "Comparison of System Stability in Distributed Power System Based on Control Method of Bus Converter", IASTED Energy and Power Systems (EPS) 2005, pp109-114.

[12] S. Abe, H. Nakagawa, M. Hirokawa, T. Zaitsu , T. Ninomiya, "System Stability of Full-Regulated Bus Converter in Distributed Power System", International Telecommunications Energy Conference (INTELEC) 2005, pp563-568.

[13] S. Abe, H. Nakagawa, M. Hirokawa, T. Zaitsu , T. Ninomiya, " Stability Improvement of Distributed Power System by Using Full-Regulated Bus Converter ", Annual Conference of the IEEE Industrial Electronics Society (IECON) 2005, pp2549-2553.

[14] S. Abe, T. Ninomiya, M. Hirokawa, T. Zaitsu , "Stability Comparison of Three Control Schemes for Bus Converter in Distributed Power System ", International Conference on Power Electronics and Drive Systems (PEDS) 2005, pp1244-1249.

[15] S. Abe, M. Hirokawa, T. Zaitsu , T. Ninomiya, " Stability Design Consideration for On-Board Distributed Power System Consisting of Full-Regulated Bus Converter and POLs ", IEEE Power Electronics Specialists Conference (PESC) 2006, pp2669-2673.

[16] R.D. Middlebrook, S. Cuk, "A General Unified Approach to Modeling Switching-Converter Power Stages," IEEE Power Electronics Specialists Conference (PESC) 1976, pp. 18-34.

[17] T. Ninomiya, M. Nakahara, T. Higashi, K. Harada, "A Unified Analysis of Resonant Converters," IEEE Transactions on Power Electronics Vol. 6. No. 2. April 1991, pp. 260-270.

[18] R. D. Middlebrook, "Input Filter Considerations in Design and Application of Switching Regulators", IAS'76, 1976, pp. 91-107.