Matrix-POL Architecture for Integrated Power Supply

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Abstract— **In this study, integrated H-bridge converter with the Matrix-POL power supply system is proposed. From the simulation results, the validity of the Matrix-POL is revealed. The results revealed that the fast response to the load current and the voltage change can be done with duty and parallel number control by the proposed system.**

Keywords— Point-Of-Load(POL), Power integrated circuit, Voltage Regulator Modules(VRM)

I. INTRODUCTION

In Fig.1, the estimation of the increased power consumption by information appliance in both of Japan and world is shown. The consumption is expected that it would be increased by 5.2 times over the period of 2006 to 2025 in Japan. Also, it is expected to be 9.4 times over the same period in the world. Japan has the plans to reduce 40% of the power consumption by 2025 [1]. Recently, Micro Processing Unit (MPU) has been required to realize energy conservation without reducing the information processing capacity [2-6]. It can be possible to perform power saving at the system level. Dynamic voltage and frequency scaling (DVFS) and power gating have been studied for MPU power conservation. DVFS is the technique that realizes the low power consumption by the optimal value of the supply voltage and clock frequency of LSI as shown in Fig.2 [7]. The power gating is the technique that suppressing the leak current by interrupting the power supply when the part of the MPU is in de-active mode in Fig.3 [8]. The concepts of these techniques were very effective for power management. But, these techniques require the tracking control for very fast change of the power supply voltage or the load current for point of load (POL) type DC-DC converter. Conventional bulky POL is not enough for achieving fast response because of the effect of the package or line impedance. Therefore, nowadays, the integration of POL with MPU has been paid attention, rapidly. In this paper, as one of the integrated POL study, Matrix-POL power supply system is proposed.

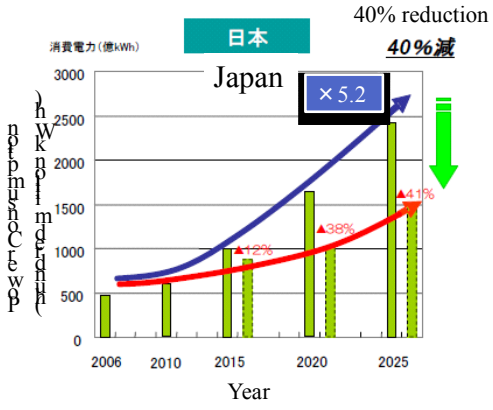
II. MATRIX-POL POWER SUPPLY SYSTEM MODEL

Recently, MPU is incorporating many cores. Each core and, further, SRAM and interface block requires independent supply voltage for energy conservation. Therefore, it is necessary to provide multiple power supply lines in the MPU. Figure 4 shows an example of proposed integrated Matrix-POL power supply system.

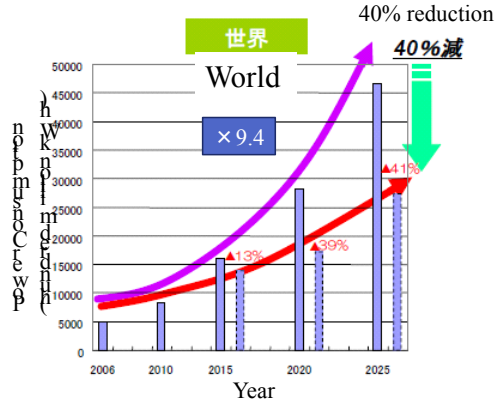
Each single POL is constructed with H-bridge converter, which has the functions of bi-directional power transfer and buck-boost voltage conversion as shown in Fig.5.

This example has two-input and m-output terminals. Each output terminal of POL is connected in parallel. The parallel number is dynamically changed by the output voltage regulation feedback control. The connection of the output terminal of each POL is realized with the power gating switches. With this technique, active series regulator can be realized by controlling the parallel number. The rest of the parallel POL is connected to the next output stage. At least, one of the terminals is connected to next output stage.

Figure 6 shows buck-mode operation and Fig.7 shows boost-mode operation of the H-bridge. The both mode is realized with just the gate control of the switches. In this paper, the simulation results are obtained just with buck-mode operation. The duty ratio of each POL in the same stage is synchronized. And the duty ratio of the each stage is adjusted with the voltage reference output (VID) of the each independent power supply blocks of MPU. VID is supplied as feed forward signal. For more detail is mentioned next chapter.



(a) Japan



(b) World

Fig.1 Changes in Estimates of Power Consumption by the Information Appliance

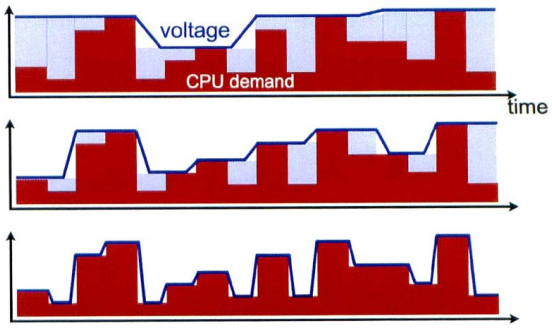


Fig.2 DVFS

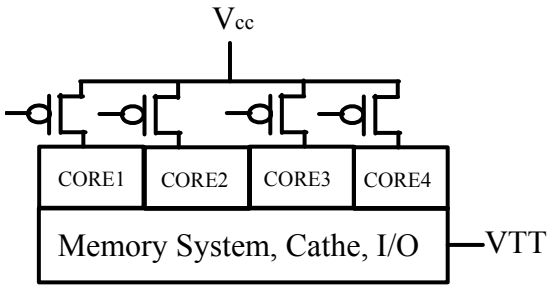


Fig.3 Power Gating

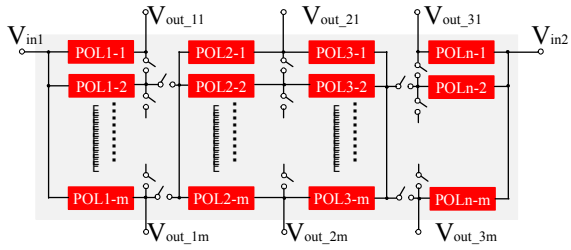


Fig.4 Matrix-POL Power Supply System

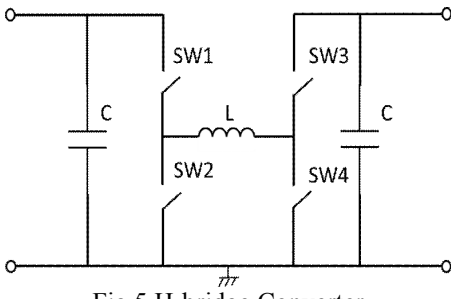


Fig.5 H-bridge Converter

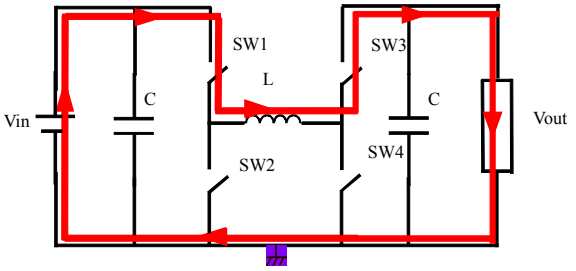
III. MATRIX-POL POWER SUPPLY SYSTEM MODEL

Figure 8 shows the control algorithm of the Matrix-POL power supply system. In this system, method of controlling the output voltage has two ways. One is the duty ratio and on the other hand is the number of parallel. In steady term, the each output terminal voltage is regulated with the feed-forward controlled duty ratio depends on VID of MPU. And, dynamical output voltage regulation is performed with feed-back controlled parallel number of POL. With this technique, high-speed-response of the output voltage is realized. Figure 9 shows simulation model. The output terminals of each ten paralleled POLs are connected to one output terminal. The gate switch can adeptly change the parallel number for the output terminal. The rest of the POLs which have not be connected to output terminal, are all connected to the input terminal of next output stage.

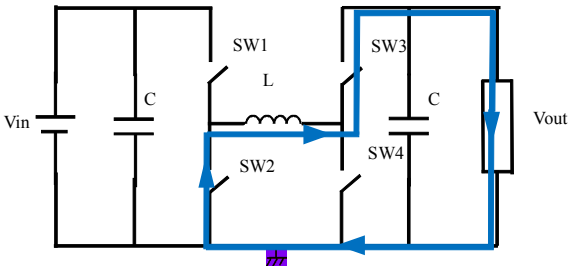
To confirm the validation of the proposed method, we performed numerical simulation for multi-output condition with Maplesim5. The Matrix-POL is configured one input voltage and three output voltage terminal. To each output voltage terminal, paralleled POL whose duty ratio is same is connected. The parallel number is dynamically changed from one to nine depends on the feed-back signal.

IV. LOAD CHAGE SIMULATIONS

To confirm the validation of the proposed method, we performed simulation for multi-output condition by Maplesim5. The Matrix-POL is configured one input voltage and three output voltage terminal. To each output voltage terminal, paralleled POL whose duty ratio is same is connected. The parallel number is dynamically changed from one to nine depends on the feed-back signal. The all of the rest parallel POL is connected to next output voltage stage. Figure 9 is simulation circuit. Square block of the figure is the H-bridge. Table I shows simulation parameters. Table II, III and IV shows the look-up-table of switch combination of terminal of output voltage 1, 2 and 3, respectively. Figure 10, 11, and 12 show simulation results of light to heavy load. Figure 13, 14 and 15 show simulation results of heavy to light load. From the results, it confirms that the output voltage is within the operating range of the load in all conditions. But there is also a part of the output voltage meets barely the operating range of the load. It is further study in this regard.

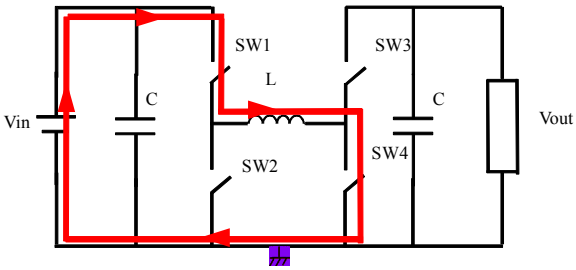


(a) Buck-mode state1

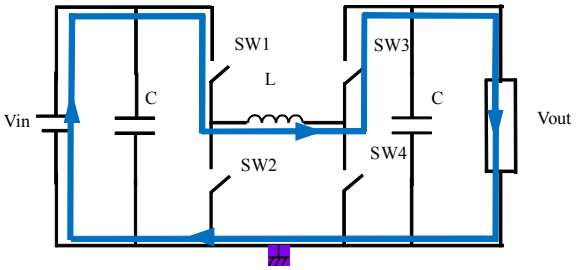


(b)Buck-mode state2

Fig.6 Buck-mode Architecture



(a) Boost-mode state1



(b) Boost-mode state2

Fig.7 Boost-mode Architecture

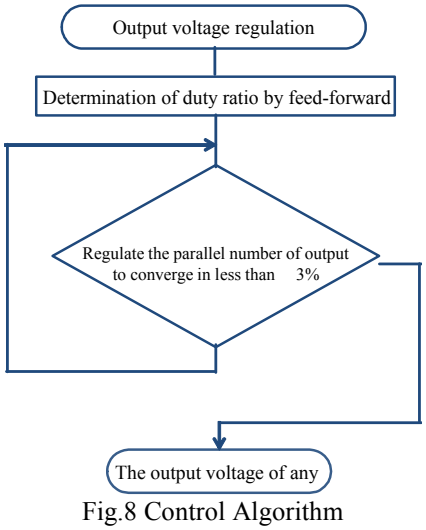


Fig.8 Control Algorithm

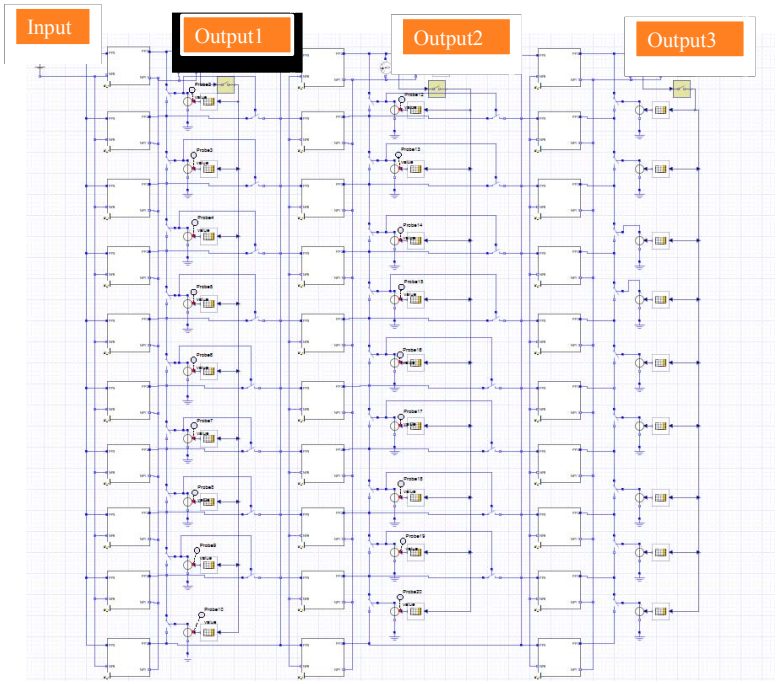


Fig.9 Simulation Circuit

Table I Simulation Parameter

Ω	
μ	
Ω	
μ	
Ω	
μ	
Ω	
Ω	

Table II Signal of Switches (Output Voltage1)

	Connection Stage								
Output Voltage1	first-second	second-third	third-fourth	fourth-fifth	fifth-sixth	sixth-seventh	seventh-eighth	eighth-ninth	ninth-tenth
0	1	1	1	1	1	1	1	1	0
4.9	1	1	1	1	1	1	1	1	0
4.9249999	1	1	1	1	1	1	1	1	0
4.925	1	1	1	1	1	1	1	1	0
4.949999	1	1	1	1	1	1	1	1	0
4.95	1	1	1	0	0	0	0	0	0
4.9749999	1	1	1	0	0	0	0	0	0
4.975	1	1	1	0	0	0	0	0	0
4.999999	1	1	1	0	0	0	0	0	0
5	1	1	1	0	0	0	0	0	0
5.001	1	1	1	0	0	0	0	0	0
5.0249999	1	1	1	0	0	0	0	0	0
5.025	1	1	0	0	0	0	0	0	0
5.0499999	1	1	0	0	0	0	0	0	0
5.05	1	0	0	0	0	0	0	0	0
5.0749999	1	0	0	0	0	0	0	0	0
5.075	0	0	0	0	0	0	0	0	0
5.1	0	0	0	0	0	0	0	0	0
100	0	0	0	0	0	0	0	0	0

Table III Signal of Switches (Output Voltage2)

Output Voltage	Connection Stage								
	first-second	second-third	third-fourth	fourth-fifth	fifth-sixth	sixth-seventh	seventh-eighth	eighth-ninth	ninth-tenth
0	1	1	1	1	1	1	1	1	0
3.2	1	1	1	1	1	1	1	1	0
3.2249999	1	1	1	1	1	1	1	1	0
3.225	1	1	1	1	1	1	1	1	0
3.249999	1	1	1	1	1	1	1	1	0
3.25	1	1	1	1	1	1	1	1	0
3.2749999	1	1	1	1	1	1	1	1	0
3.275	1	1	1	1	1	1	1	1	0
3.2999999	1	1	1	1	1	1	1	1	0
3.3	1	1	0	0	0	0	0	0	0
3.3000001	1	1	0	0	0	0	0	0	0
3.3249999	1	1	0	0	0	0	0	0	0
3.325	1	1	0	0	0	0	0	0	0
3.3499999	1	1	0	0	0	0	0	0	0
3.35	1	0	0	0	0	0	0	0	0
3.3749999	1	0	0	0	0	0	0	0	0
3.375	0	0	0	0	0	0	0	0	0
3.4	0	0	0	0	0	0	0	0	0
100	0	0	0	0	0	0	0	0	0

Table IV Signal of Switches (Output Voltage3)

	Connection Stage								
Output Voltage	first-second	second-third	third-fourth	fourth-fifth	fifth-sixth	sixth-seventh	seventh-eighth	eighth-ninth	ninth-tenth
0	1	1	1	1	1	1	1	1	0
1.4	1	1	1	1	1	1	1	1	0
1.4249999	1	1	1	1	1	1	1	1	0
1.425	1	1	1	1	1	1	1	1	0
1.449999	1	1	1	1	1	1	1	1	0
1.45	1	1	1	1	1	1	1	1	0
1.4749999	1	1	1	1	1	1	1	1	0
1.475	1	1	1	1	1	1	1	1	0
1.4999999	1	1	1	1	1	1	1	1	0
1.5	1	1	0	0	0	0	0	0	0
1.5000001	1	0	0	0	0	0	0	0	0
1.5249999	1	0	0	0	0	0	0	0	0
1.525	1	0	0	0	0	0	0	0	0
1.5499999	1	0	0	0	0	0	0	0	0
1.55	1	0	0	0	0	0	0	0	0
1.5749999	1	0	0	0	0	0	0	0	0
1.575	0	0	0	0	0	0	0	0	0
1.6	0	0	0	0	0	0	0	0	0
100	0	0	0	0	0	0	0	0	0

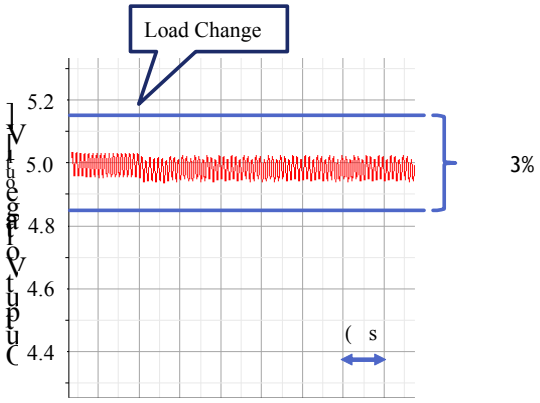


Fig.10 Output Voltage (Light to Heavy)

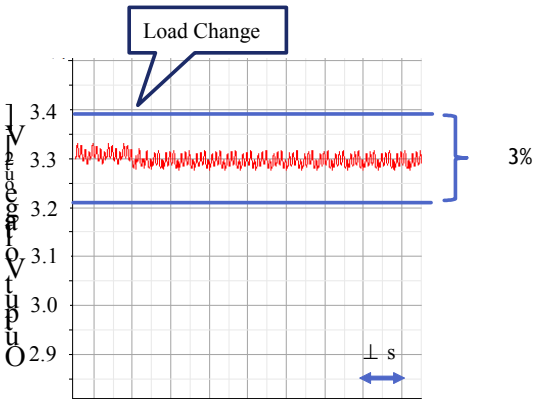


Fig.11 Output Voltage (Light to Heavy)

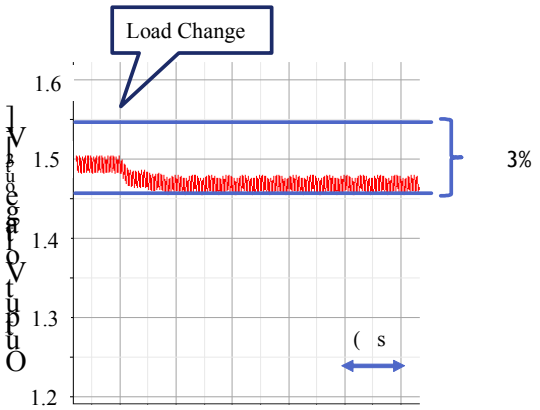


Fig.12 Output Voltage (Light to Heavy)

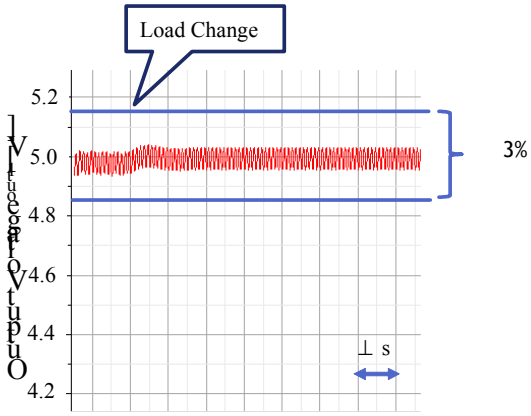


Fig.13 Output Voltage (Heavy to Light)

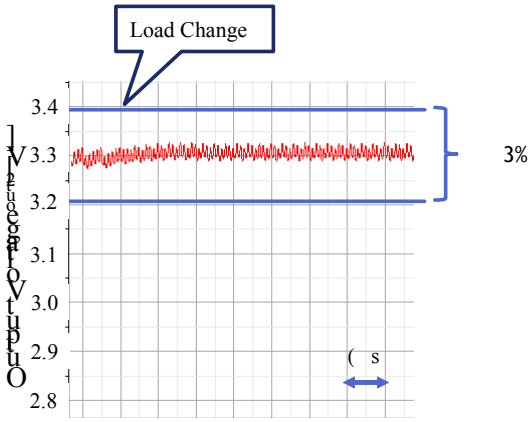


Fig.14 Output Voltage (Heavy to Light)

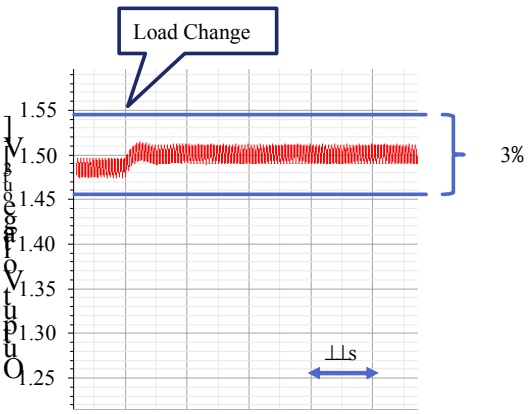


Fig.15 Output Voltage (Heavy to Light)

V. CONCLUSIONS

In this paper, Matrix-POL architecture for integrated power supply is proposed. From the simulation results, the validity of the Matrix-POL is shown. The results revealed that the fast response to the load current and the voltage change can be done with duty and parallel number control.

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