Sub-microsecond Response Digital Controller for POL

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***Abstract*—This paper will discuss about the proposed hard-ware logic type digital controller for on-board SMPS which has a very small time-delay in control loop. Some experimental has been done including estimation of the load current change experiment and the frequency characteristic of open loop transfer function. These result reveal the proposed circuit could be suppressed the time delay to sub-microsecond order. To use the multi-phase system reduces the output ripple.**

Keywords—DPWM,Point of Load(POL),Digital Control ,Multi-Fhase

I. INTRODUCTION

Digital electronic products have been spreading quickly by the advancement of the integrations technologies. ICs, DSPs and FPGAs require a high performance and a high speed due to the trend. Along with the situations, the power consumption is increasing. To suppress the power consumption, the power supply voltage is getting lower toward to sub 2V. Figure 1 shows the relation between size of LSI and margin of V_{DD}. The trend of future size of LSI and margin of V_{DD} are going to become lower and more severe. Because of the severe voltage margin by the lower power supply voltages, special SMPS, point of load (POL) is disposed very near to the load. The requirements of the control circuit of POL are high accurate, high speed, adaptive and low cost. For the control purpose, pulse width modulation (PWM) control is a one of appropriate technique. Digital control or DPWM can accomplish robust and flexible power control with soft-tuned parameters and will become popular control technique. Although, there are some disadvantages in cost and speed, against analog control circuit. Proposed hardware-logic based digital PWM control circuit is effective to such requirements.

In this paper, trend and problems of DPWM controller for POLs is introduced at first. At the next, the proposed DPWM control method's principles of operation and circuit configurations are described. At last, the effectiveness of the proposed technique is confirmed with some experiments and comparison between prior works and prototype proposed circuit is introduced.

II. DPWM CONTROL METHOD FOR POL

A. Current State of DPWM Controller for POL

Before describing the proposed digital control system for POL, trend of digital controllers for POLs are summarized. The trend is categorized with some keywords, which are treated in these papers [2]-[21] that treat DPWM control, in Fig. 2.

We have found that most of the paper treats the transient response performance, small size and power consumption. In contrast, the cost has not been discussed so much. But this point cannot be ignored because the cost is also important in the real electronic products.

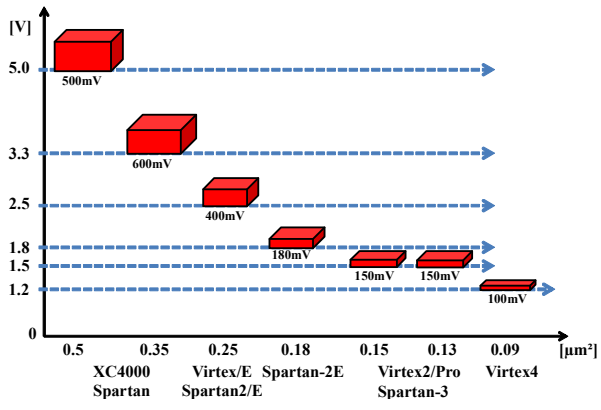


Fig. 1 The relation between size of LSI and margin of V_{DD}

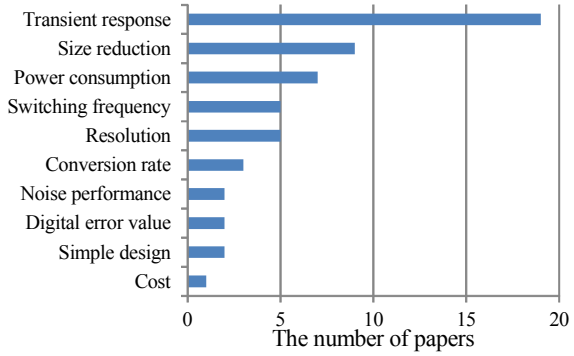


Fig.2 Key point of DPWM controller and number of papers

Therefore, designing good DPWM controller, is taking balance of all of the factors including the cost. .

In the next section, the problems about the restrict factor of high-speed response of DPWM control are described.

B. The Circuit Configuration of General DPWM Controller for POL

The circuit configuration of general DPWM controlled POL is shown in Fig.3(a). This topology has two major time-delay problem. First, time-delay occurs at A/D converter with the conversion-delay. And, the calculation time of digital controller is another problem. Both of the time-delay directly effects on the response speed of the control circuit and influences stability of the control. Total of the delay time will be described as the discrete delay factor e^{-Ls} in the control loop shown in Fig.3(b). In general, total of the delay time is 600nsec at least excepting the delay time of driver circuit.

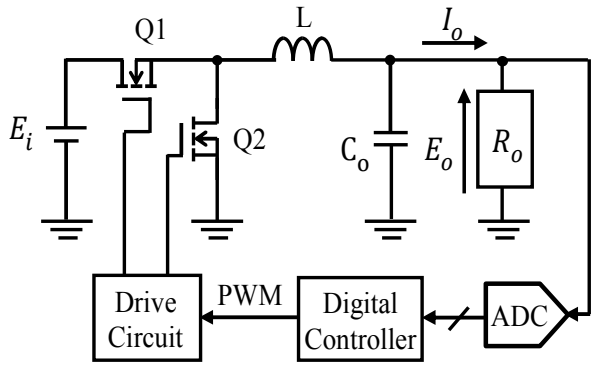
C. The Circuit Configratin of Proposed DPWM Controller for POL

Main POL circuit is a quite ordinary non-isolated buck converter. The control circuit is composed with D/A converter, analog comparator, digital controller and drive circuit.

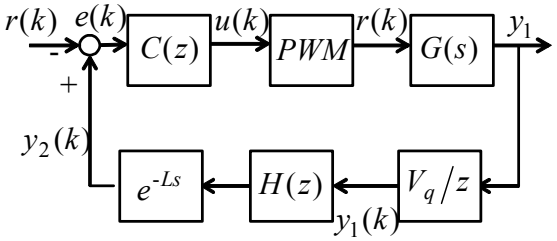
The analog timing converter (ATC) block shown in Fig.4(a) is composed with D/A converter and analog comparator. In Fig.4(b), the control block diagrams are shown. ATC block, PID control calculation block and up-counter block for gate pulse creation, are all in parallel and synchronized with the system clock f_{CLK}.

D. The control circuit configuration of the proposed DPWM-POL

Figure 5 shows the precise control circuit configuration, and Fig. 6 shows control signal flow of the proposed DPWM-POL. Let's take a look at the signal flow.

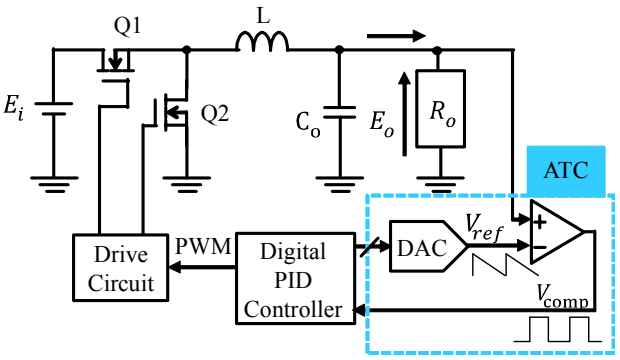


(a) Circuit configuration

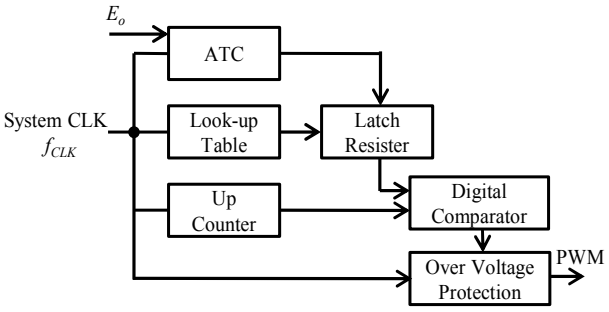


(b) Control block

Fig.3 General DPWM-POL



(a) Proposed DPWM-POL



(b) Control block

Fig.4 Circuit configuration of proposed DPWM-POL

As mentioned above, all blocks are synchronized with the system clock f_{CLK}. Memory 1 is used the look-up table method, and can store waveform values not only triangle or saw tooth but any waveforms. In this paper, the step-down saw tooth wave form is employed. V_{ref}^{+} is the maximum output voltage of DAC. The output voltage E_o of POL is compared with the output voltage of D/A converter in the ATC block, successively. The comparator's output is read out to the latch signal to each D-ff at the timing that E_o was sensed. Also, the look-up table method is used for the duty ratio calculation with memory 2, 3 and 4. Especially, the duty ratio data which is pre-calculated with the value of E_o, are stored in memory 2.

The duty ratio data is read out from memory2 according to f_{CLK}. At the timing of E_o sensed, one of the duty ratio data is chosen and transferred to $u(k)$ in D-ff4, where k is the number of switching term.

Because of the small delay of this control technique, the sensed E_o data can reflect on-term of the same switching term.

At the digital comparator, $u(k)$ is compared with up-counter data, and converted to real-time analog PWM waveforms. On-term $T_{on}(k)$ of DPWM signal of switching term k is decided by $u(k)$. In parallel with the processing of ATC block, the $u(k)$ is called with system clock and latched by ATC output as trigger. At the last of the switching term, $u(k)$ is preset maximum value by PR signal generator for preparing next term.

The delay of the proposed control circuit is mostly dominated with the calling and the loading time of memory 2.

E. PID control with Look-up Table

$u(k)$ which is stored in memories is pre-calculated by general PID digital control laws as

$$u(k)=u_{ref}+K_P e(k)+K_I n_I(k)+K_D(e(k)-e(k-1)) \qquad (1)$$

where u_{ref} is a reference value of $u(k)$, $e(k)$ is an digitalized error value between r which is digitalized reference voltage V_{ref} and, $y_1(k)$ is output data of up-counter in switching term k as

$$e(k) = y_1(k) - r \qquad (2)$$

K_P, K_I and K_D are a proportional gain, an integral gain and an derivative gain, respectively, $n_I(k)$ is integral factor, that is

$$n_I(k) = n_I(k-1) + e(k) \qquad (3)$$

At the timing of the latch signal is becoming high, $y_1(k\text{-}1)$ is latched to $y_2(k\text{-}1)$ as

$$y_2(k-1) = y_1(k-1) \qquad (4)$$

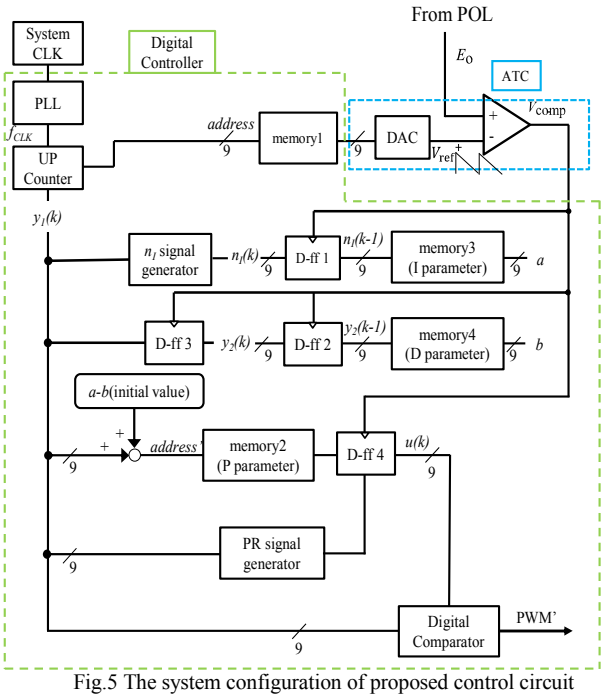


Fig.5 The system configuration of proposed control circuit

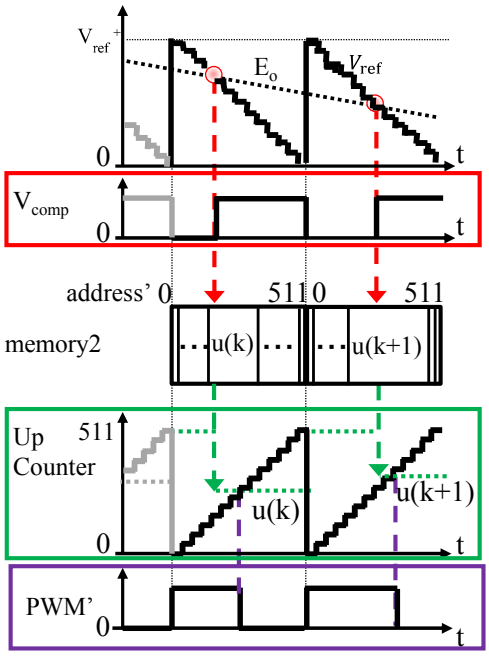


Fig.6 Control signal flow

TABLE I Address and data of memory2 at $K_P = 5, K_I = 0$

address	memory2	
0	0	nonlinear
1	0	
...	...	
22	0	
23	1	linear
24	6	
25	11	
26	16	
...	...	
119	481	
120	486	
121	491	
122	496	
123	500	nonlinear
...	...	
511	500	

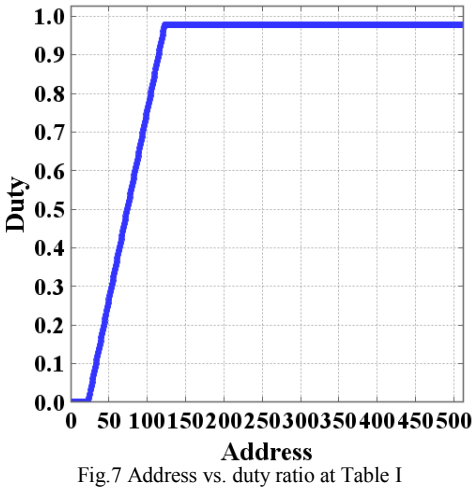


Fig.7 Address vs. duty ratio at Table I

From above equations, (1) can be transformed to

$$u(k)=u_{ref}-(K_P+K_I)r+A\{y_1(k)+\frac{K_I}{A}n_I(k-1)-\frac{K_D}{A}y_2(k-1)\} \quad (5)$$

Where

$$A=K_P+K_I+K_D \quad (6)$$

$$a=\frac{K_I}{A}n_I(k-1) \quad (7)$$

$$b=\frac{K_D}{A}y_2(k-1) \quad (8)$$

Memory 3 and memory 4 store *a* and *b,* respectively.

In (5), $a-b$ in the term *k* is pre-calculated in the term *k-1* and the obtained value becomes the initial value of programmable counter of the term *k*. And, *address'* which indicates address of memory 2 is incremented with system clock and *u(k)* is called from memory 2, simultaneously.

$$address'=y_1(k)+a-b \quad (9)$$

From (5) and (9),

$$u(k)=u_{ref}-(K_P+K_I)r+A\{address'\} \quad (10)$$

Therefore, *u(k)* is determined as soon as E_o is sensed.

Table I shows the address and data of memory2 at $K_P=5, K_I=0$, u_{ref}=86, r= 40 in (10). Figure 6 shows address and duty ratio at Table I. You can see, Table I data have linear and nonlinear domain. And, if K_P becomes more higher, linear domain becomes shorter.

F. Overvoltage protection logic circuit

If trigger does not occur, proposed circuit outputs overvoltage. Therefore, we use overvoltage protection logic circuit.

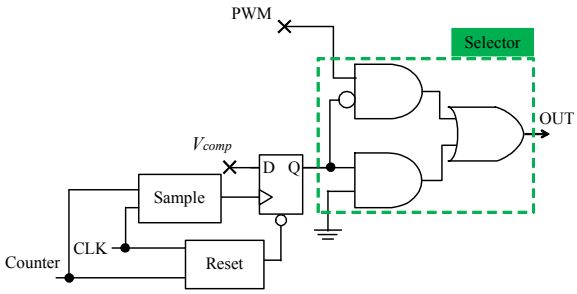


Fig.8 The system configuration of overvoltage protection logic circuit

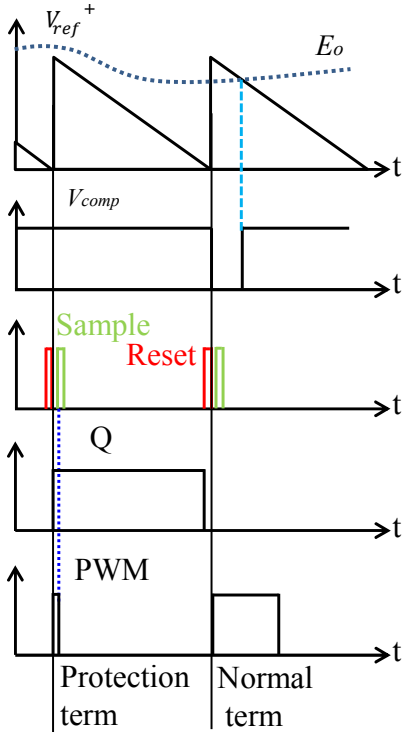


Fig.9 Protection signal flow

Table II Truth table of selector of protection logic circuit

Q	OUT
0	PWM
1	Gnd

Figure 8 shows overvoltage protection circuit for proposed circuit. It is composed with selector, D-ff, sample pulse generator and reset pulse generator for D-ff.

Figure 9 shows protection signal flow, and Table II shows truth table of the selector. First, sample pulse generator occurs pulse, second, value of Q is decided by sample pulse and V_{comp}, at last OUT is decided by Table II. When sensed output voltage $E_o > V_{ref}^+$, PWM signal becoming off by force.

G. *The proposed circuit with Multi-phase method*

Figure 10 shows the main and the proposed control circuit configuration using a multi-phase method. The circuit is composed of five-phase.

There are some benefits to use multi-phase converter. For example, multi-phase converter is able to supply stable output current for increasing of load current because of reducing of current per phase than single-phase and reduction of ripple current. By some factors mentioned above, transient response is improved. Therefore, it has become an effective method in recently. However, there are some disadvantages that increasing of cost and circuit scale, difficulty of control by increasing of the switching element than single-phase. Therefore, appropriate design is needed to compensate above disadvantages. In proposed control system, multi-phase converter is designed easily.

Figure.11 shows how to adopt the multi-phase method to the proposed circuit. The signal flow of multi-phase system block is shown in Fig.12. These figures show how to recognize system block of second-phase.

Timing of the falling edge of PWM2 signal is determined by that of PWM signal which is first-phase. First, the timing of the rising edge of the PWM2 signal is determined by the block of Start in Fig.11. Duty ratio of PWM2 is created by adding two values of counter which are the timing of PWM falling edge and PWM2 rising edge. Block of Const creates constant value which is same value of PWM2 rising. In this time, it is 102. Q of D-ff I and output of block of Const are added by Adder block. At block of Phase, output of Adder and value of counter are compared. And the just timing of the value of counter becomes equal to output of Adder, 0 is output form Phase block. Output of Phase block can reset output of D-ff II and determine the falling edge of PWM2 signal.

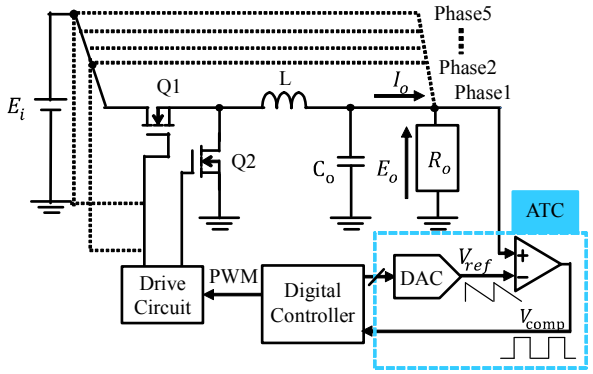


Fig.10 Proposed circuit with multi-phase

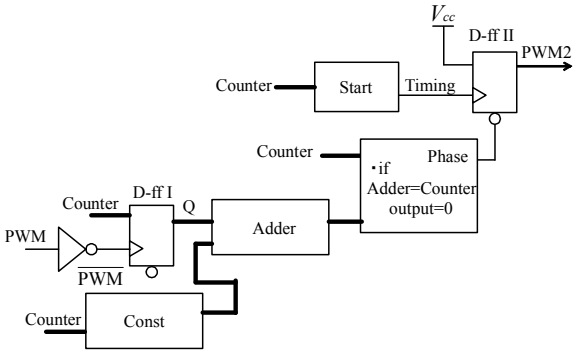


Fig.11 The system configuration of logic circuit with multi-phase method

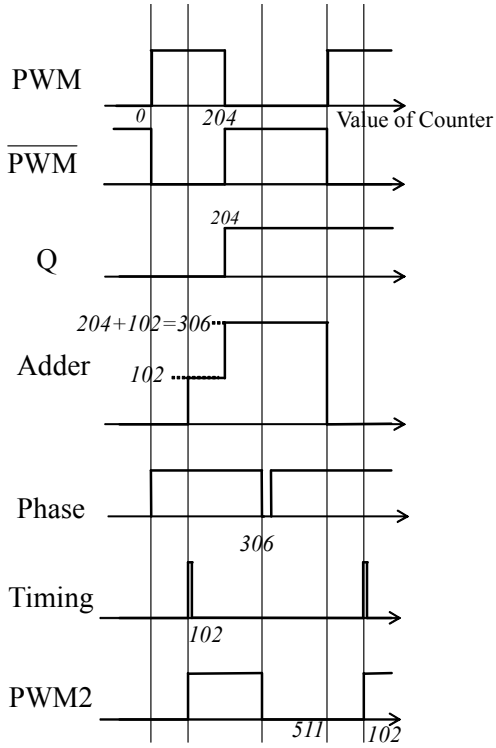


Fig.12 Signal flow of proposed circuit with multi-phase

III. EXPERIMENTAL RESULTS

A. *Specifications*

The proposed control system with prototype circuit is shown in Fig.13. The digital controller part is designed with FPGA Altera Cyclone IV. Texas Instruments DAC900 is used as DAC. Linear Technology LT1719 is used as analog comparator. FDMF6705V is used as MOSFEET and driver. The DC-DC converter topology is basically same as buck converter in Fig.4(a). The buck converter with proposed controller was verified with the experimental conditions are shown in Table III. The experimental conditions with multi-phase are shown in Table IV.

B. *Experimental set-up*

Some experiments are performed to verify the proposed controller. Figure.14 shows experimental set-up of load current change dynamic response. We measured output voltage E_o ,V_{comp},PWM signal and output current I_o with analog probe , V_{comp} and $u(k)$ in Fig.5 with digital probe. Current change slew rate is 50A/μs.

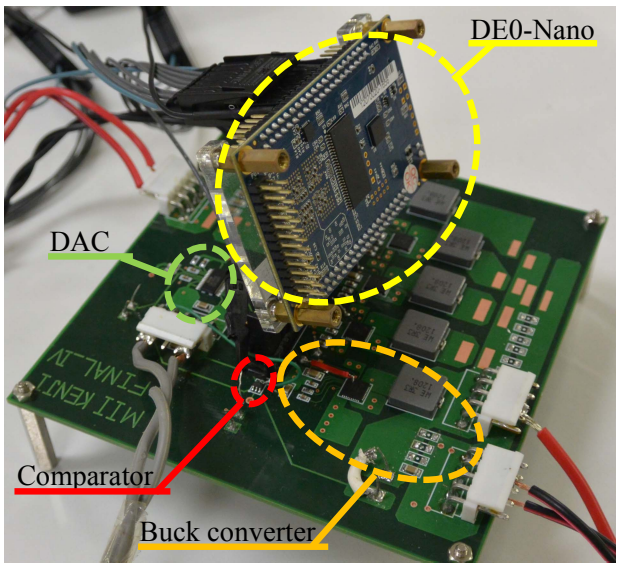


Fig.13 Prototype circuit

TABLE III

Parameters / Components	Value / name
Input voltage E_i	12V
Output target voltage	1.5V
Output current I_o per phase	0.3A ~ 0.9A
Switching frequency f_s	1MHz
Choke inductor L	3.3μH
Output capacitor C_o	10μF(single)/57μF(five)
Proportional gain K_P	10
Integral gain K_I	0
Differential gain K_D	0
V_{ref}^{+}	1.6
f_{CLK}	500MHz
Current change slew rate	50A/μs
Digital PWM resolution	9bit
Dr. MOS (MOSFET and driver)	Fairchild FDMF6705V
Analog comparator	Linear Technology LT1719
D/A converter	Texas Instruments DAC900
FPGA	Terasic DE0-Nano (Cyclone IV)

C. Measurement Results

1) Static characteristics

Figure 15 shows static characteristic at KP=10. It shows when load current with single-phase is 0.3~0.9, output voltage is 3% of target voltage.

2) Load current change transient response

Figure 15 and 16 show experimental waveforms of load current change transient response. Both figures show E_o: 100mV/div(CH1), PWM: 3V/div(CH2), V_{comp}: 3V/div(CH3), I_o: 1A/div (CH4), V_{comp} (digital):D9, $u(k)$:D0-D8, respectively. Bottom figure is an enlargement of a part of top figure and it shows reflection time. Figure 16 and 17 show 0.3~0.9A load transient response at K_P=10. Figure 16 shows light to heavy load transient response and output voltage settled in 10.4μs, under shoot is 160mV. Figure 17 shows heavy to light load transient response and output voltage settled in 3.2μs, over shoot is 58mV. From these figures, the reflection time from sensed V_{comp} to $u(k)$ change is 11.0ns even in the worst case.

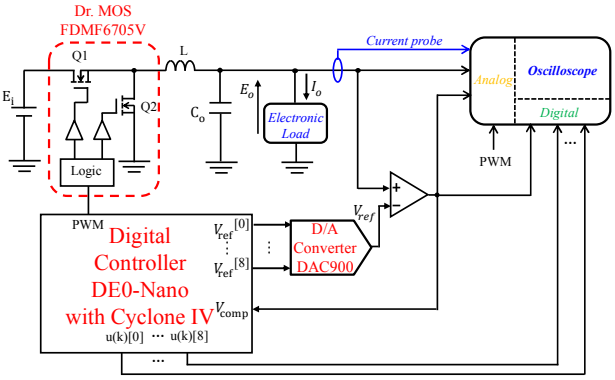


Fig. 14 Experimental set-up ststic characteristic and load current change transient response

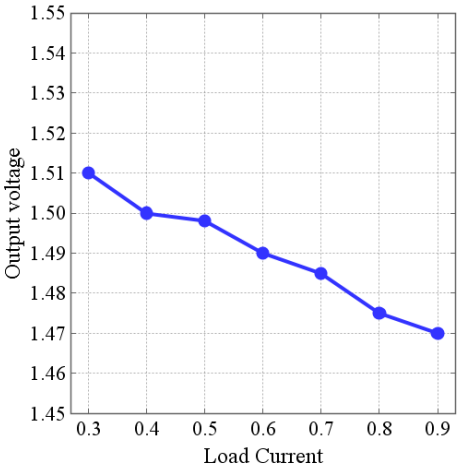


Fig. 15 Static characteristic of converter at K_P=10

Table IV is comparing the settling time of the output voltage from the proposed digitally controlled switching converter with prior work. It shows that the proposed digital controller achieves faster output settling time than existing digital controller.

1) Load current change transient response with multi-phase method

Fig18 and 19 show experimental waveforms of load current change transient response using multi-phase method. Measurement range used in this experiment is the same as single-phase. They are 0.3~0.9A load transient response at K_P=10. Figure 18 shows light to heavy load transient response and output voltage settled in 15.6μs, under shoot is 190mV. Figure 19 shows heavy to light load transient response and output voltage settled in 9.0μs, over shoot is 170mV.

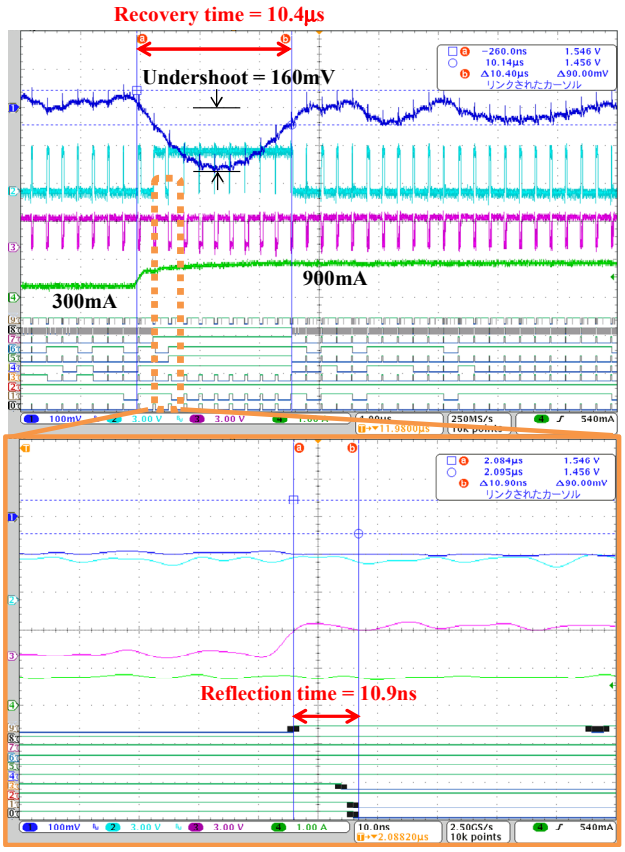


Fig. 16 Load change from 0.3 to 0.9A (K_P=10)

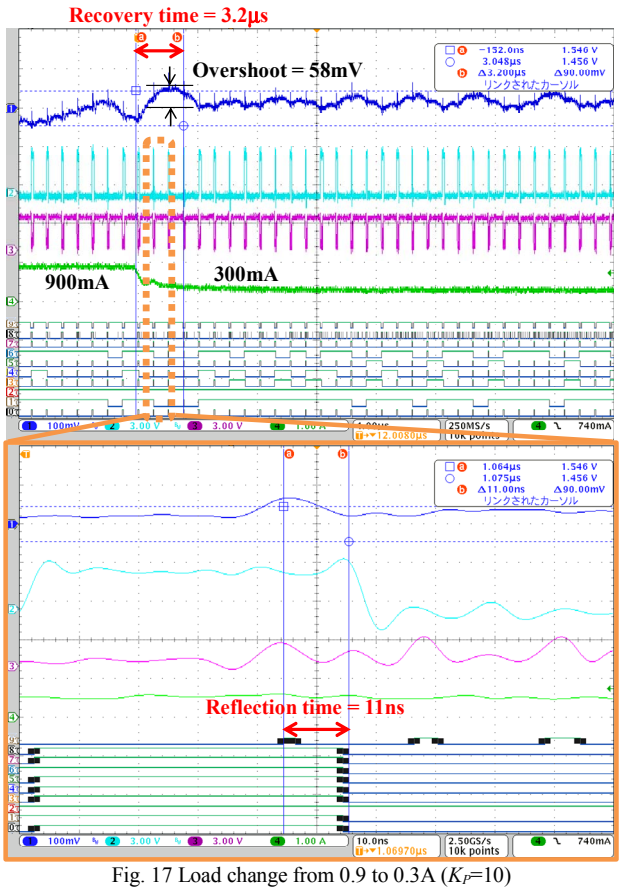


Fig. 17 Load change from 0.9 to 0.3A (K_P=10)

TABLE IV COMPARISON WITH PRIOR WORKS.

	[18]	[19]	[20]	[21]	This work
L	10μH	4.7μH	4.7μH	4.7μH	3.3μH
C	10μH	4.7μH	4.7μH	22μF	10μF
Switching frequency	1M	4M	1M	780k	1M
Load Current step	0.45A	0.16A	0.6A	0.59A	0.6A
Input voltage	1.8 -3.8V	3.3V	3V	3.6V	12V
Output target voltage	1.2V	1.5V	1.8V	1.2V	1.5V
Settling time	3.5μs	18μs	15.5μs	60μs	10.4μs

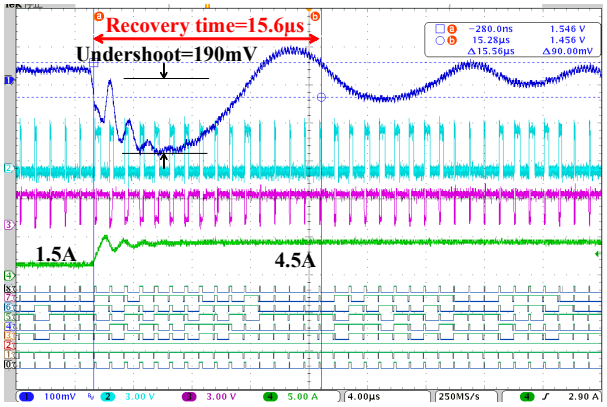


Fig18 Load change with multi-phase 1.5A to 4.5A (K_P=10)

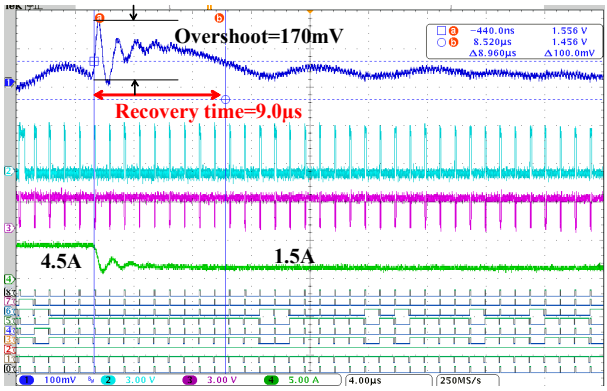


Fig.19 Load change with multi-phase 4.5A to 1.5A (K_P=10)

IV. CONCLUSIONS

In this paper, the hardware logic type digital controller for on-board SMPS, which has a very small time-delay in control loop, is confirmed with some experiments including frequency characteristic. In single-phase, settling time of proposed prototype circuit is 10.4 μs, and undershoot is 160 mV. This result with the specifications of table III is superior in DPWM-POLs. And the reflection time from sensed V_{comp} to $u(k)$ change is 11.0ns even in the worst case. The total reflection time of control system except driver circuit is in 50n sec. Therefore, it is confirmed that the proposed circuit is able to respond sub-microsecond. In addition, multi-phase proposed

circuit achieved reduction of the output ripple. Settling time is 15.6μs and undershoot is 190mV. From these results, it is confirmed that the proposed circuit can increase output current stably by using multi-phase. As the future work, to further enhance the PID control added to the integral control and to devise new control system, such as can be achieved faster.

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